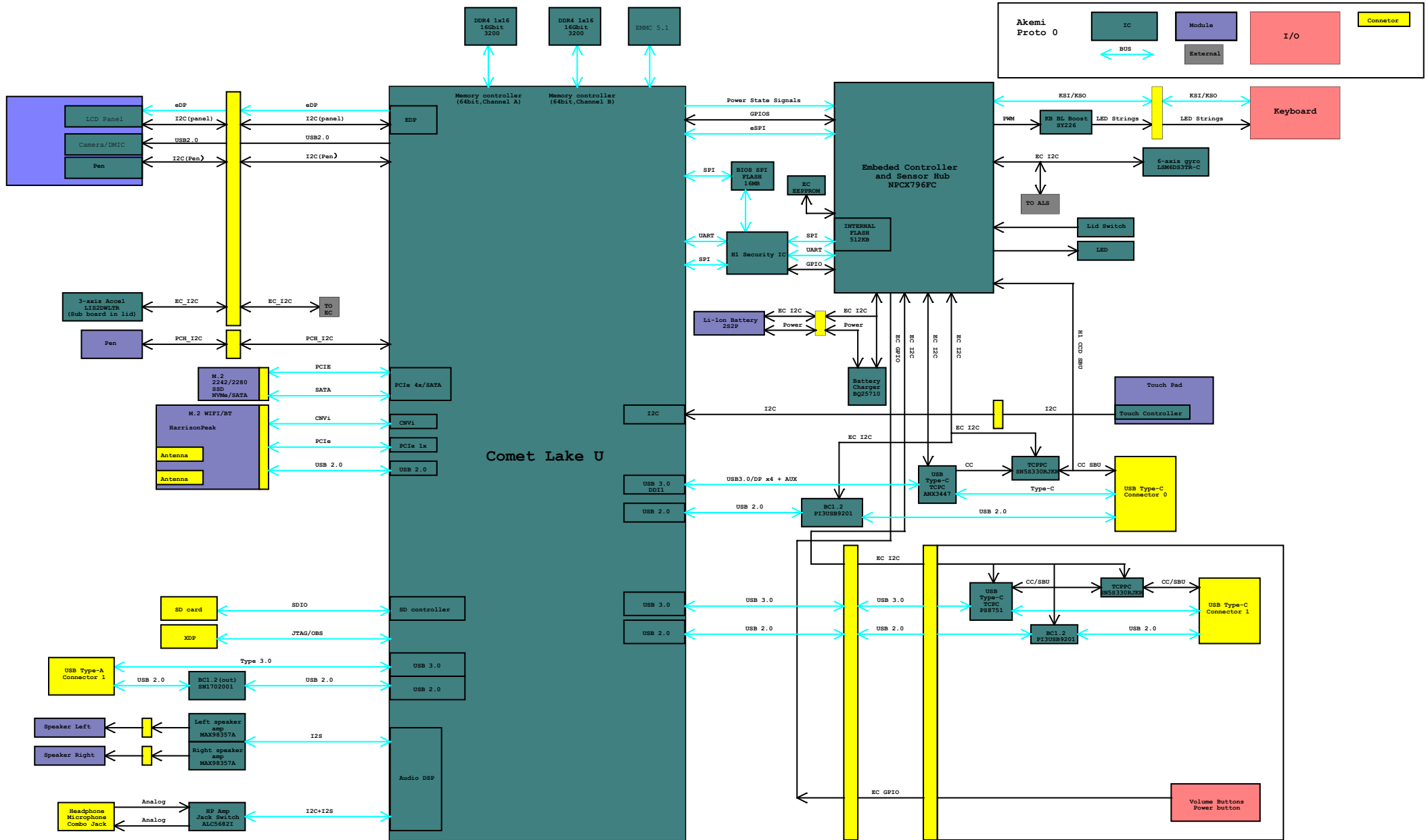
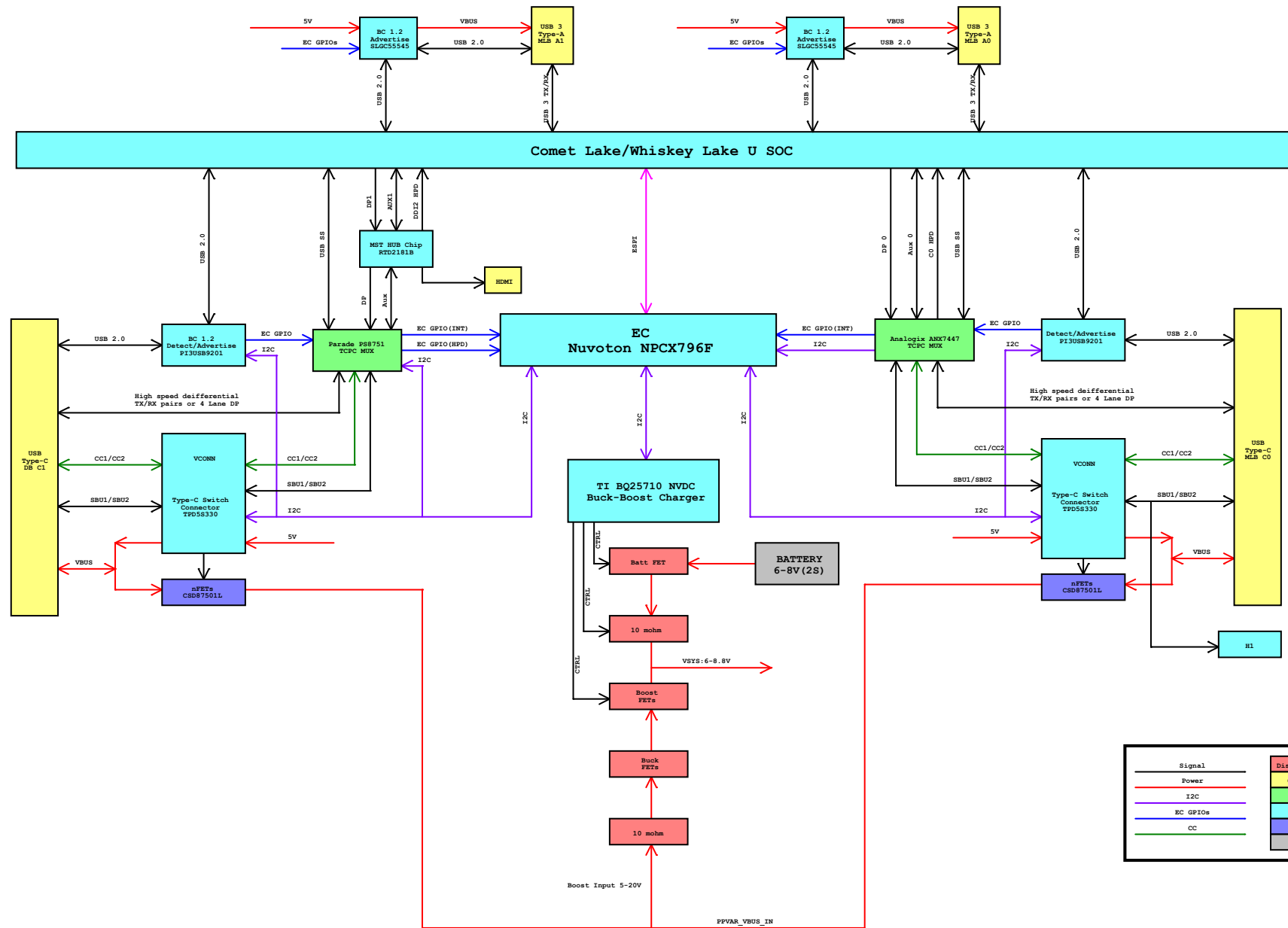


SCH: 650-03895-01-SCH  
ASSY: 650-03895-01  
PCB: 651-03895-01

SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	TYPE-C BLOCK DIAGRAM
4	POWER TREE
5	POWER SEQUENCING
6	I2C MAP
7	CML: MEMORY
8	CML: DISPLAY
9	CML: USB/PCIE
10	CML: AUDIO/SD/EMMC/CNVI
11	CML: ESPI/SPI/UART/I2C
12	CML: POWER SEQ
13	CML: CORE POWER
14	CML: PCH POWER
15	CML: GND
16	CML: DEBUG/RSVD
17	CML: POWER RAIL DECOUPLING
18	MEMORY CH A-1 DDR4
19	MEMORY CH A-2 DDR4
20	MEMORY CH B-1 DDR4
21	MEMORY CH B-2 DDR4
22	MEMORY DECOUPLING/TERM
23	SPI ROM
24	H1
25	XDP DEBUG HEADER
26	SERVO DEBUG
27	eMMC/SSD M.2
28	AUDIO: SPEAKER AMPS
29	AUDIO: HEADPHONE AMP
30	BASE: KB, TP, FAN, LED

[illegible]







PPVAR\_SYS

PP3300\_G(EC/H1)

PP3300\_TCPC\_G  
PP3300\_EC

PP5000\_A

PP3300\_A

PP1800\_A

PPVAR\_VPPIM\_CORE\_A

PP1050\_A

EC\_PCH\_RSMRST\_L  
(DSW\_PWROK/RSMRST#)

EC\_PCH\_PWR\_BTN\_ODL  
(PWRBTN#)

SLP\_S4\_L

PP2500\_DRAM\_U

PP1200\_DRAM\_U

PP600\_DRAM\_U

SLP\_S3\_L

PP1050\_ST\_S

PP950\_VCCIO

SLP\_S0\_L

CPU\_C10\_GATED\_L

PP1200\_PLLOC\_S0

PP1050\_STG\_S0

VCCST\_PG\_OD  
(VCCST\_PWRGD)

PG\_EC\_ALL\_SYS\_PWRGD  
(ALL\_SYS\_PWRGD)

EC\_PCH\_SYS\_PWROD  
(SYS\_PWROD)

PPVAR\_SA

IMVP8\_VRRDY\_OD  
(VR\_READY)

PCH\_PWEOK

PLT\_RST\_L

Enabled by PPVAR\_VSYS

Enabled by EC when not in standby

Enabled by EC(at same time as 3.3A)

Enabled by PP3300\_A\_PG

Enabled by PP1800\_A\_PG

Enabled by VPRIM\_CORE\_A\_PG\_OD

Generated by logic

Enabled by SLP\_S4\_L

Enabled by SLP\_S4\_L with 2ms delay

Enabled by VTT\_CTRL

Enabled by SLP\_S3\_L OR XDP\_OVERRIDE

Enabled by SLP\_S3\_L AND VDDQ\_PG AND PP1050\_ST\_S\_PG

Rises with PP3300\_A

Rises with PP3300\_A

Enabled by CPU\_C10\_GATED\_L AND SLP\_S3\_L

Enabled by CPU\_C10\_GATED\_L AND SLP\_S3\_L

VCCST AND SLP\_S3\_L AND VDDQ\_PG AND VCCIO

VCCST AND SLP\_S3\_L AND VDDQ\_PG AND VCCIO 2ms delay

VCCST AND SLP\_S3\_L AND VDDQ\_PG AND VCCIO programmable delay Generated by EC

Enabled by ALL\_SYS\_PWRGD,SVID

ALL\_SYS\_PWRGD AND VR\_READY

16ms delay

Power Rail

Signal from PCH

Signal from Platform

# Hatch I2C Map

Updated:11/07/2018

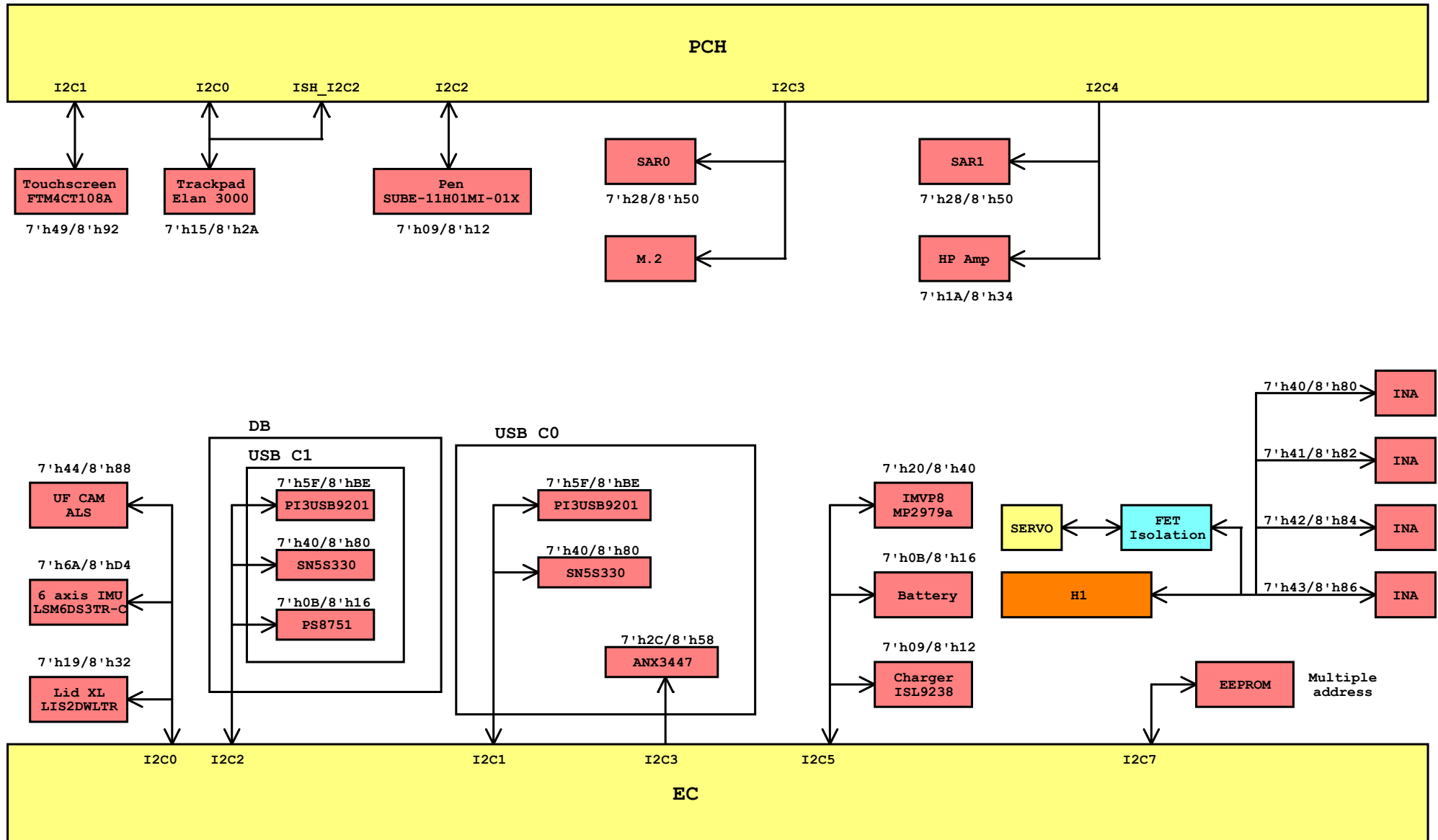
## LEGEND

I2C Master & Slave

I2C Master

I2C Slave

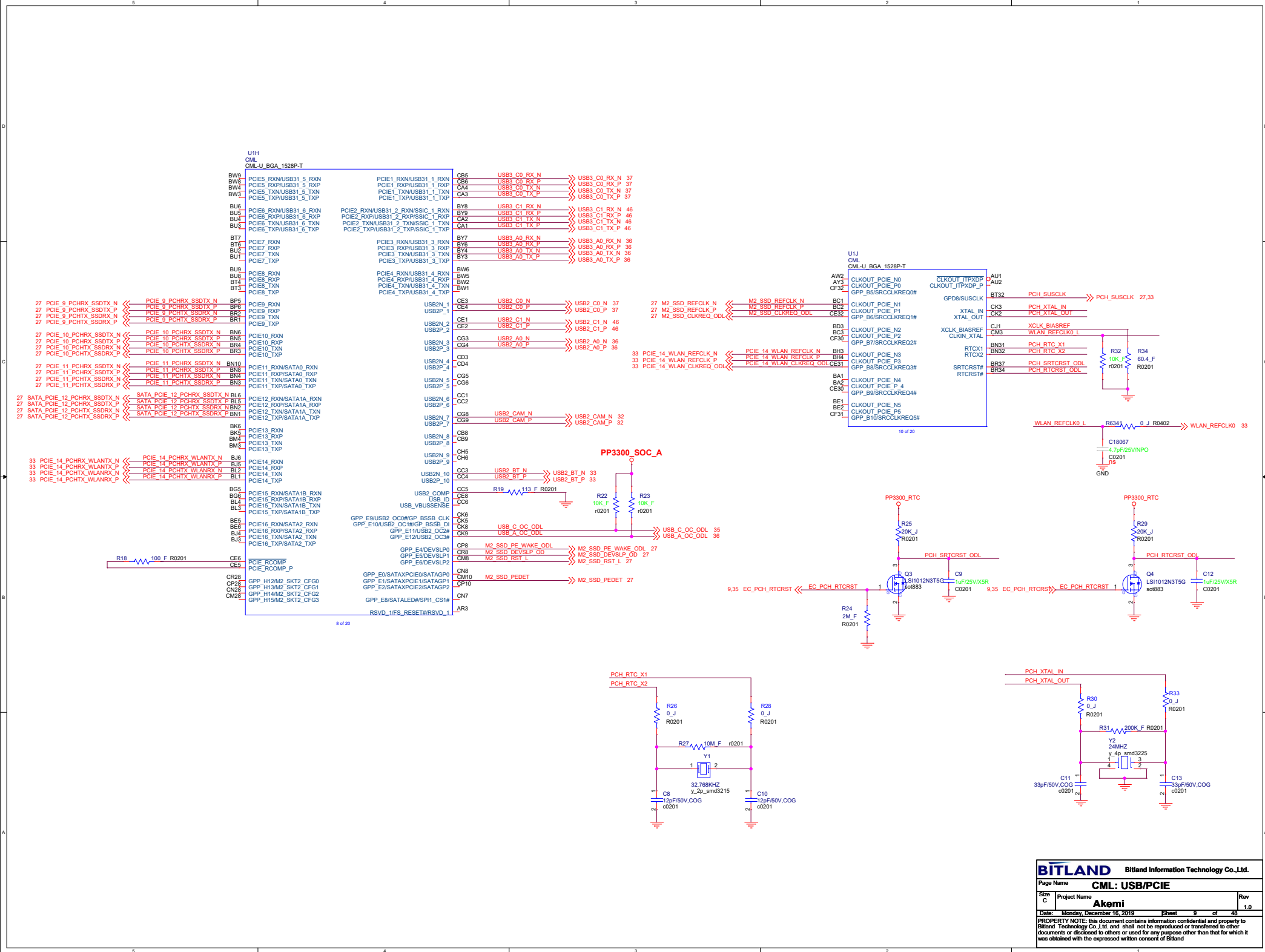
I2C addresses given in both 7 and 8 bit forms

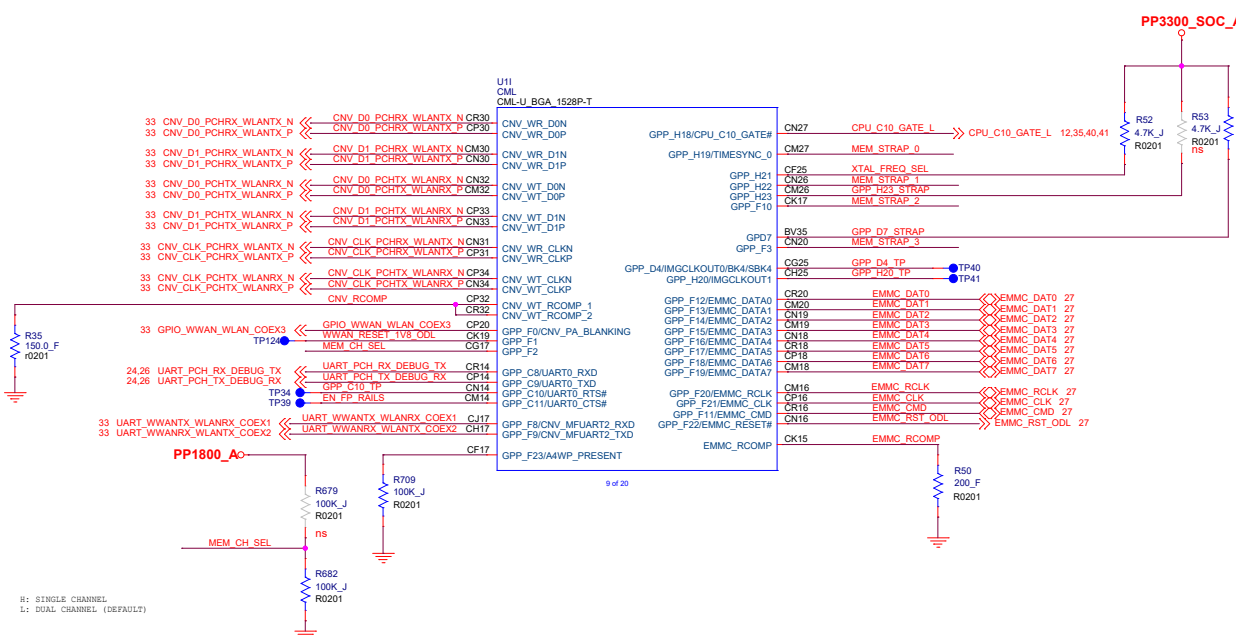




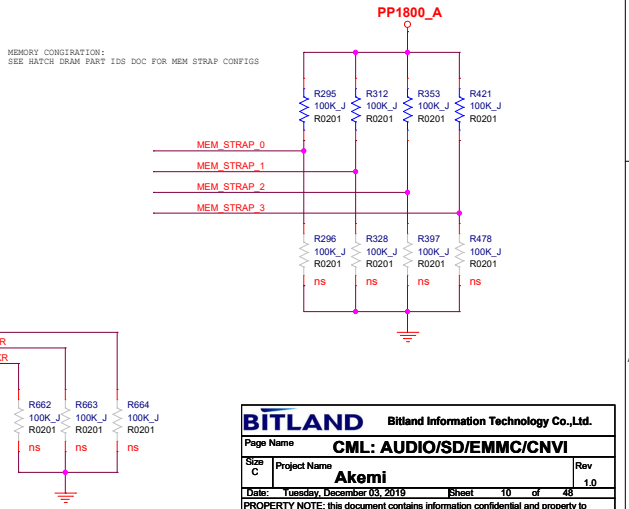
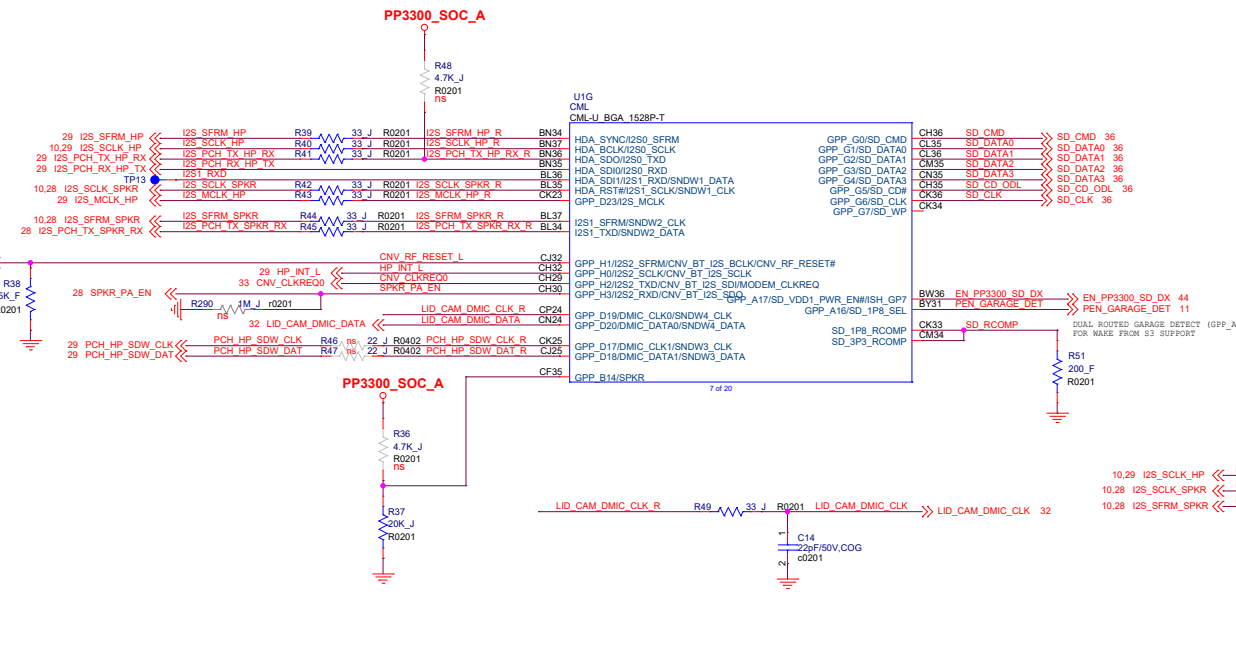








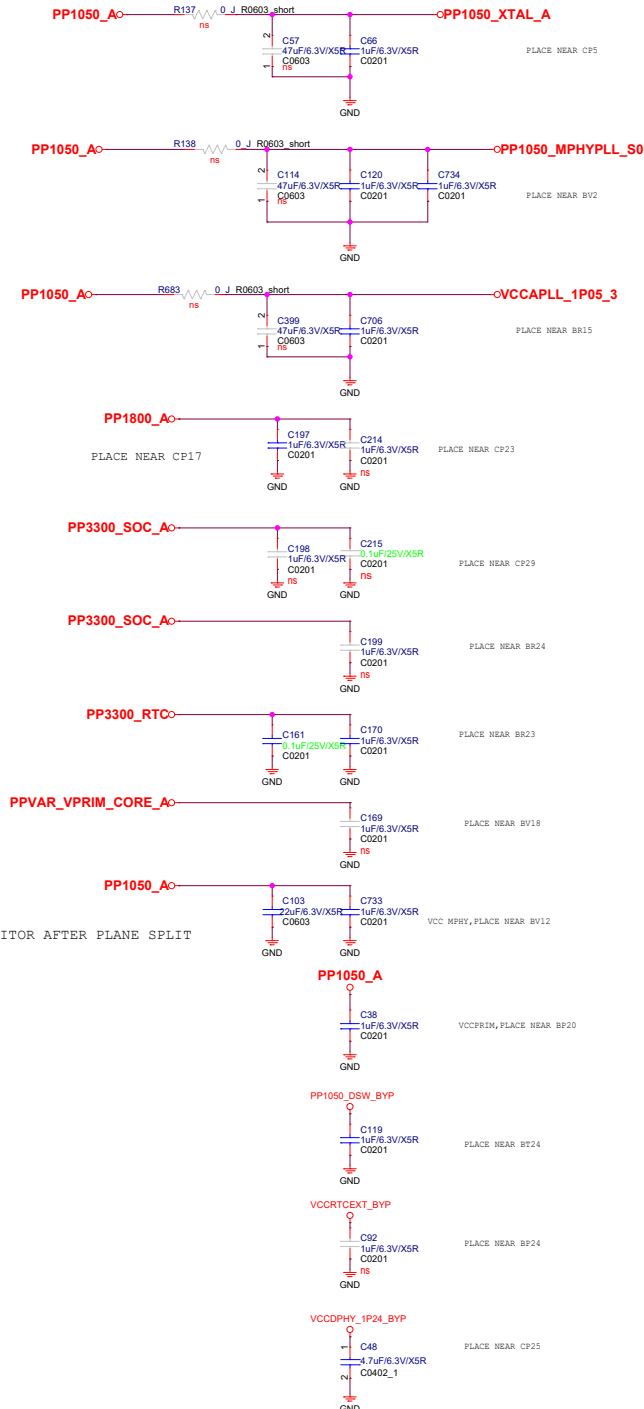
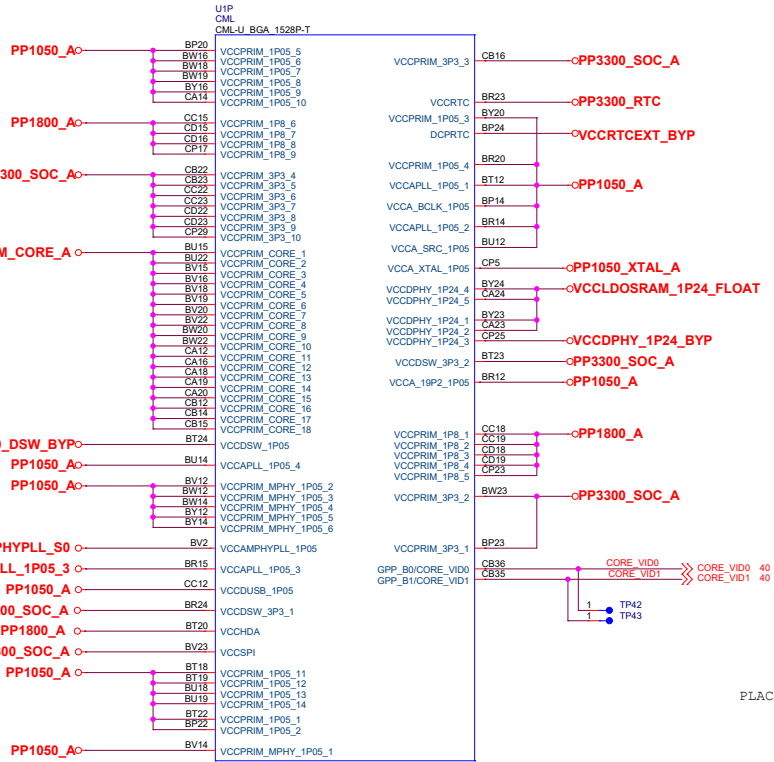
HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)	
GPP_B14: EXTERNAL PD * DISABLE TOP SWAP MODE: 0 ENABLE TOP SWAP MODE: 1	GPP_E19: INTERNAL PD DISPLAY PORT B NOT DETECTED: 0 * DISPLAY PORT B DETECTED: 1
GPP_B18: INTERNAL PD * DISABLE NO REBOOT MODE: 0 ENABLE NO REBOOT MODE: 1	GPP_E21: INTERNAL PD DISPLAY PORT C NOT DETECTED: 0 * DISPLAY PORT C DETECTED: 1
GPP_C2: INTERNAL PD * DISABLE TSL CIPHER SUITE: 0 ENABLE TSL CIPHER SUITE: 1	GPP_E23: INTERNAL PD * DISPLAY PORT D NOT DETECTED: 0 DISPLAY PORT D DETECTED: 1
GPP_B22: INTERNAL PD * BOOT BIOS FROM SPI: 0 BOOT BIOS FROM LPC: 1	GPP_H23: MAF VS SAF SEL * MASTER ATTACHED FLASH: 0 SLAVE ATTACHED FLASH: 1
GPP_C5: INTERNAL PD LPC IS SELECTED FOR EC: 0 * ESPI IS SELECTED FOR EC: 1	GPP_F6 (M2 CAED CONTROLLED) INTEGRATED CNVI ENABLE: 0 *INTEGRATED CNVI DISABLED: 1
SPIO_MOSI EXTERNAL PU REQUIRED	SPIO_IO2 EXTERNAL PU REQUIRED
GPD7 EXTERNAL PU REQUIRED	SPIO_IO3 EXTERNAL PU REQUIRED
GPP_B23: INTERNAL * DISABLE DCI-OOB: 0 ENABLE DCI-OOB: 1	HDA_SDO: INTERNAL PD * ENABLE FLASH DESCRIPTOR SECURITY: 0 DISABLE FLASH DESCRIPTOR SECURITY: 1
INPUT3VSEL * 3.3V SUPPLY IS 3.3V: 0 3.3V SUPPLY IS 3.0V:	GPP_H21: XTAL FREQ SEL XTAL FREQ IS NOT 24MHZ: 0 *XTAL FREQ IS 24MHZ: 1
GPP_D12 EXTERNAL PU REQUIRED	ITP_MODE INTERNAL PU, MUST SAMPLE HIGH
GPP_H17 INTERNAL PD, MUST SAMPLE LOW	

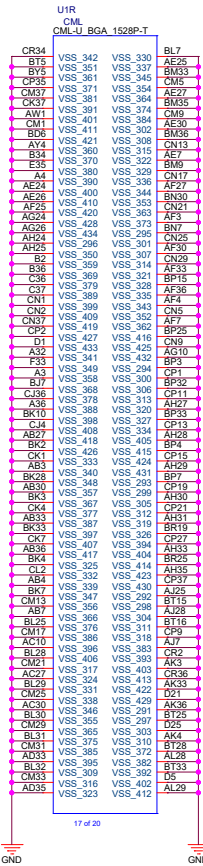




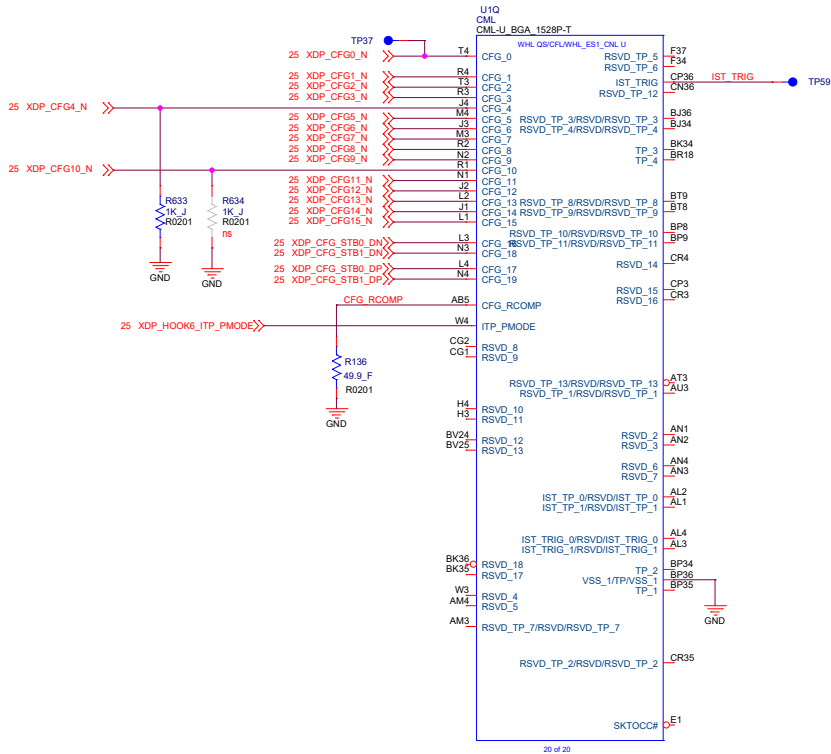




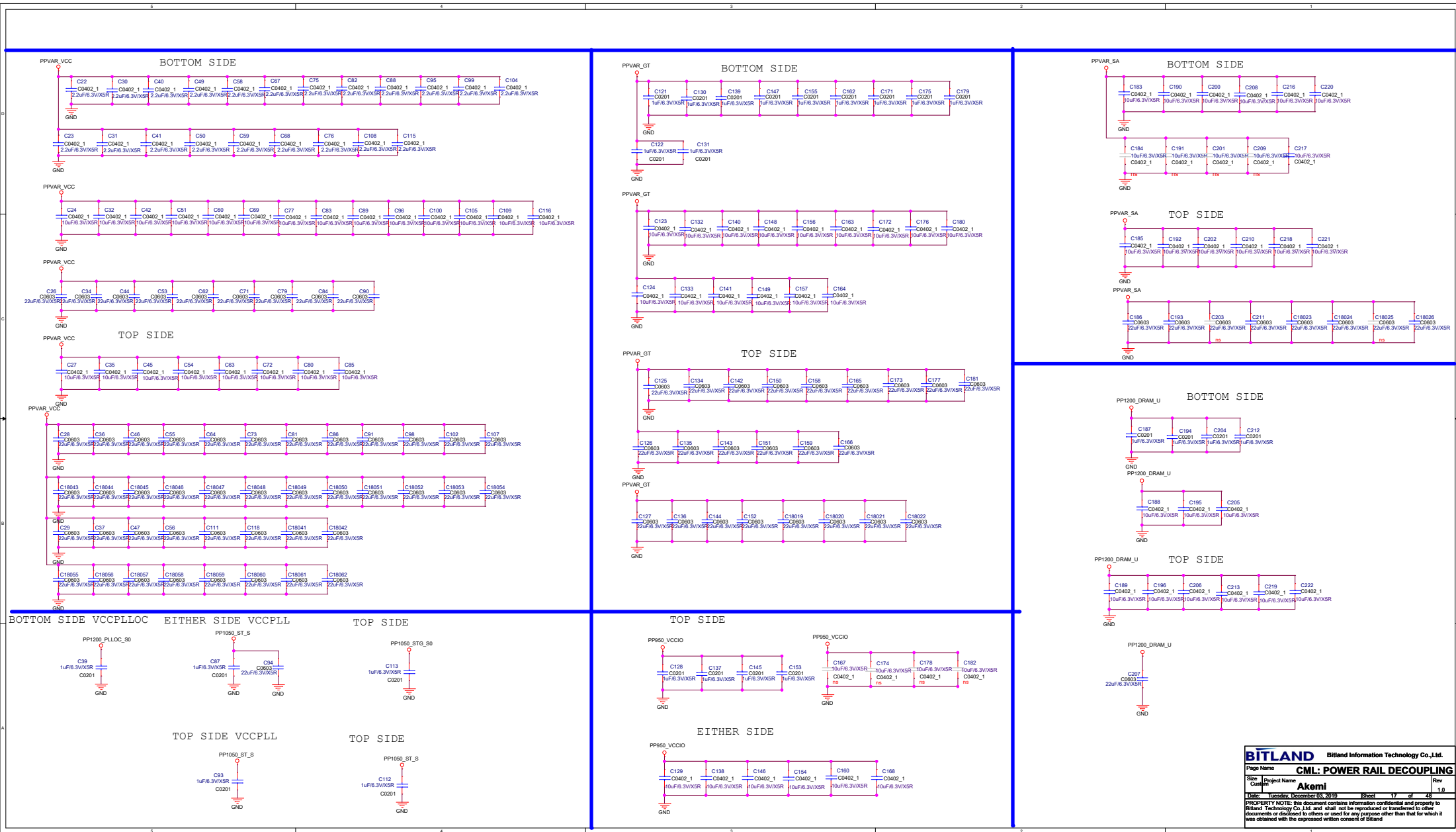


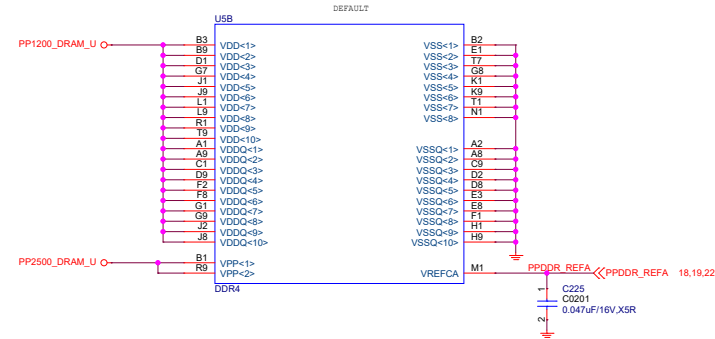
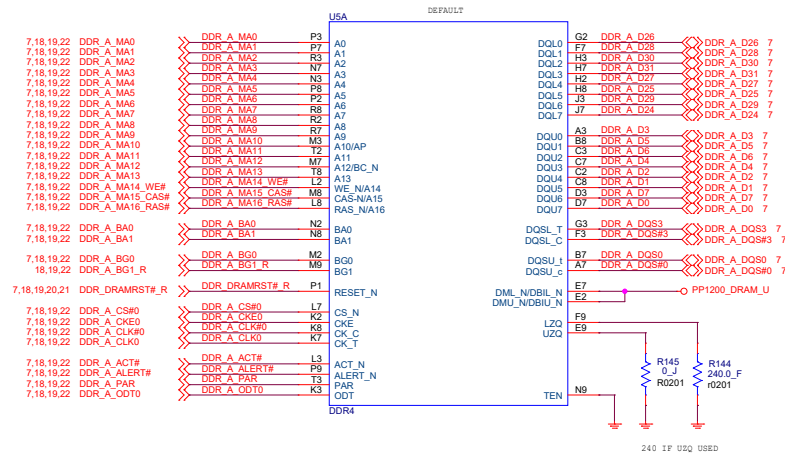
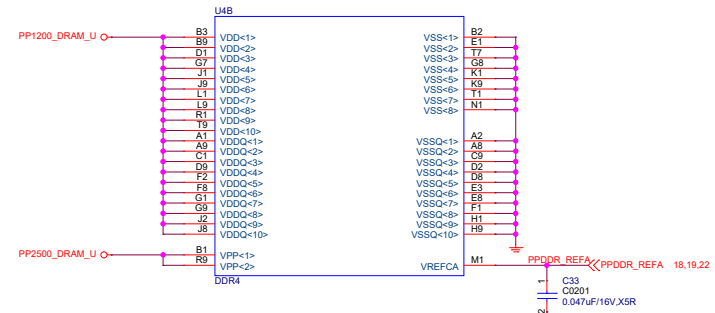
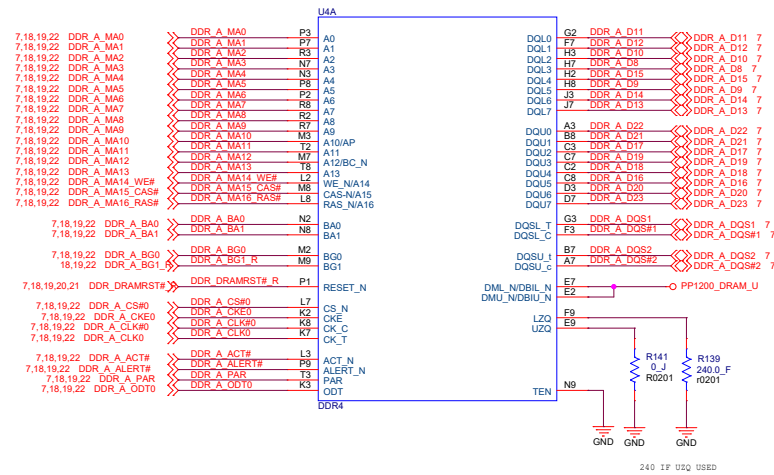


U10	CML	CML-U BGA 1528P-T
K12	WHL QSICFL/UWHL_E81 ONL U22	WHL QSICFL/UWHL_E81 ONL U22
K14	RSVD_25/VCC_OPC_1/RSVD_25	RSVD_39/VCCCEPIO_1/RSVD_39
K15	RSVD_26/VCC_OPC_2/RSVD_26	RSVD_40/VCCCEPIO_2/RSVD_40
K17	RSVD_27/VCC_OPC_3/RSVD_27	RSVD_41/VCCCEPIO_3/RSVD_41
K18	RSVD_28/VCC_OPC_4/RSVD_28	RSVD_42/VCCCEPIO_4/RSVD_42
K20	RSVD_29/VCC_OPC_5/RSVD_29	RSVD_43/VCCCEPIO_5/RSVD_43
L25	RSVD_30/VCC_OPC_6/RSVD_30	RSVD_44/VCCCEPIO_6/RSVD_44
M24	RSVD_31/VCC_OPC_7/RSVD_31	RSVD_45/VCCCEPIO_7/RSVD_45
M26	RSVD_32/VCC_OPC_8/RSVD_32	RSVD_46/VCCCEPIO_8/RSVD_46
P24	RSVD_33/VCC_OPC_9/RSVD_33	RSVD_47/VCCCEPIO_9/RSVD_47
P26	RSVD_34/VCC_OPC_10/RSVD_34	RSVD_48/VCCCEPIO_10/RSVD_48
R24	RSVD_35/VCC_OPC_11/RSVD_35	RSVD_49/VCCCEPIO_11/RSVD_49
R26	RSVD_36/VCC_OPC_12/RSVD_36	RSVD_50/VCCCEPIO_12/RSVD_50
V24	RSVD_37/VCC_OPC_13/RSVD_37	RSVD_51/VCCCEPIO_13/RSVD_51
V25	RSVD_38/VCC_OPC_14/RSVD_38	RSVD_52/VCCCEPIO_14/RSVD_52
Y24	RSVD_39/VCC_OPC_15/RSVD_39	RSVD_53/VCCCEPIO_15/RSVD_53
Y25	RSVD_40/VCC_OPC_16/RSVD_40	RSVD_54/VCCCEPIO_16/RSVD_54
G2	RSVD_41/VCC_OPC_17/RSVD_41	RSVD_55/VCCCEPIO_17/RSVD_55
G1	RSVD_42/VCC_OPC_18/RSVD_42	RSVD_56/VCCCEPIO_18/RSVD_56
C34	RSVD_43/VCC_OPC_19/RSVD_43	RSVD_57/VCCCEPIO_19/RSVD_57
G3	RSVD_44/VCC_OPC_20/RSVD_44	RSVD_58/VCCCEPIO_20/RSVD_58
G4	RSVD_45/VCC_OPC_21/RSVD_45	RSVD_59/VCCCEPIO_21/RSVD_59
A34	RSVD_46/VCC_OPC_22/RSVD_46	RSVD_60/VCCCEPIO_22/RSVD_60
B35	RSVD_47/VCC_OPC_23/RSVD_47	RSVD_61/VCCCEPIO_23/RSVD_61
AJ27	RSVD_48/VCC_OPC_24/RSVD_48	RSVD_62/VCCCEPIO_24/RSVD_62
AH26	RSVD_49/VCC_OPC_25/RSVD_49	RSVD_63/VCCCEPIO_25/RSVD_63
L5	RSVD_50/VCC_OPC_26/RSVD_50	RSVD_64/VCCCEPIO_26/RSVD_64

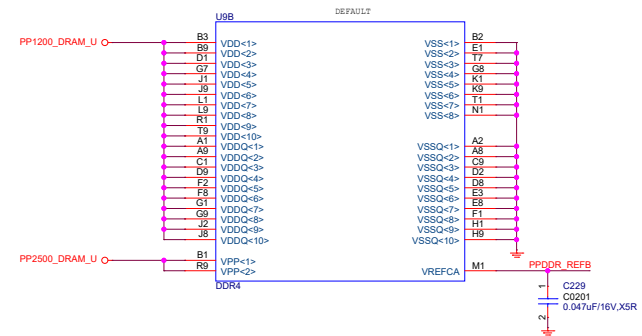
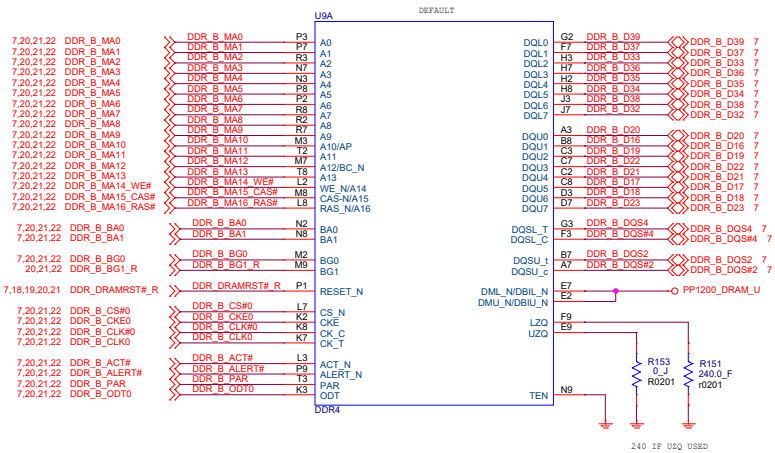
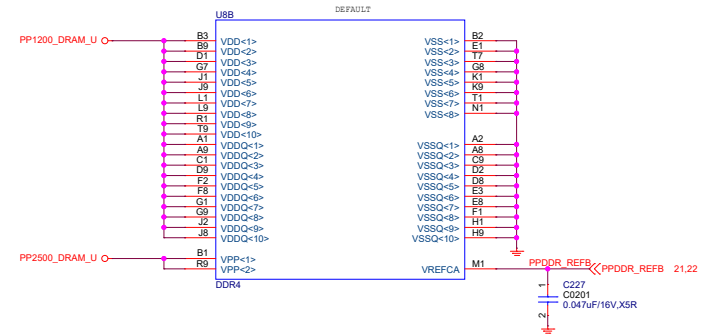
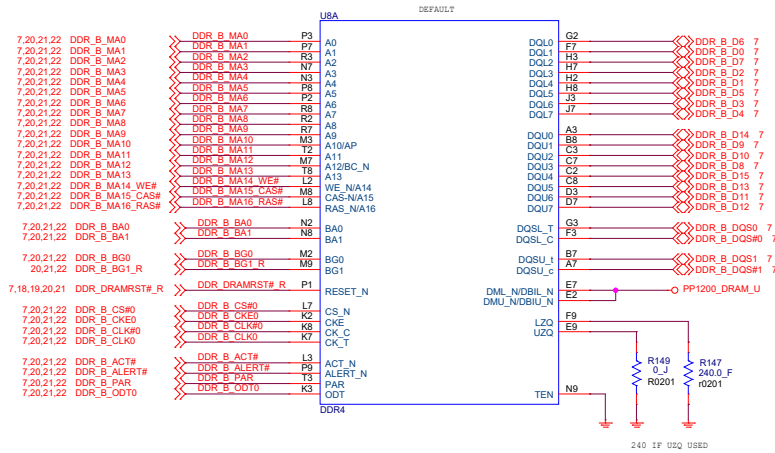


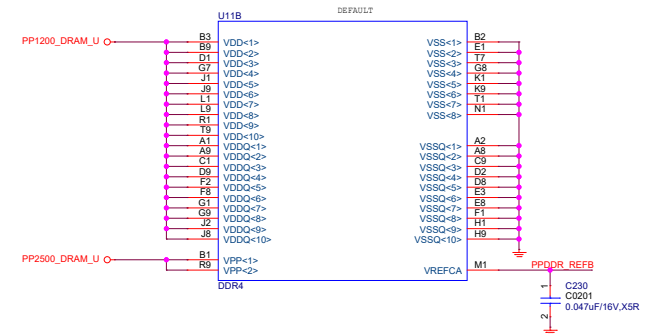
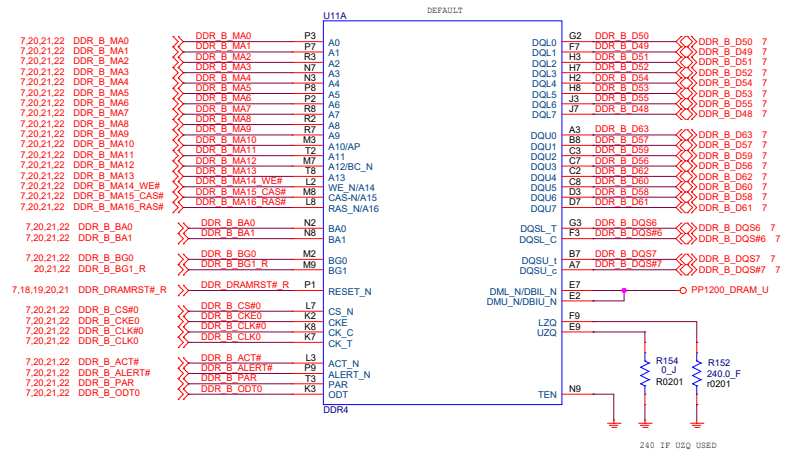
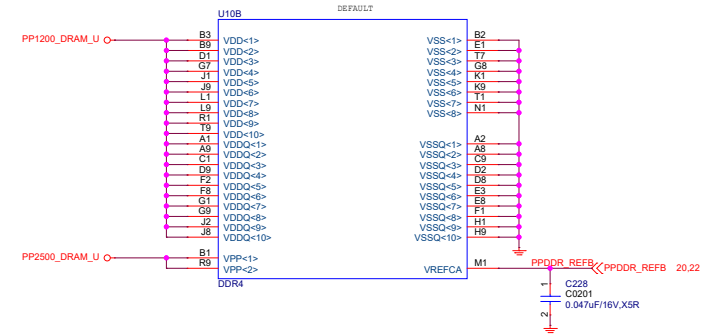
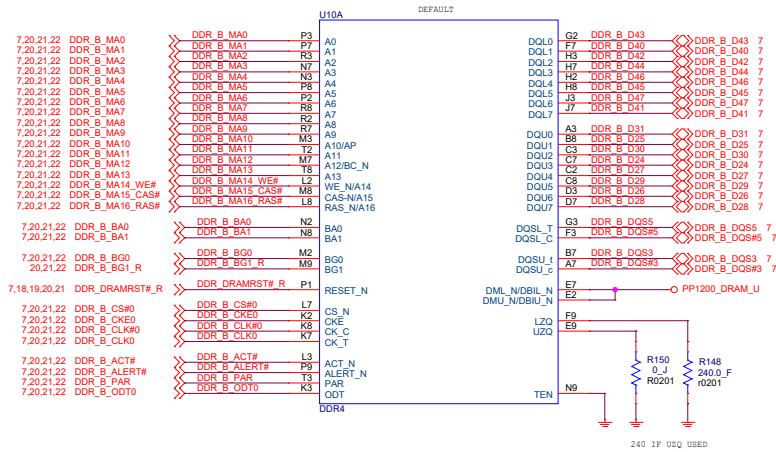




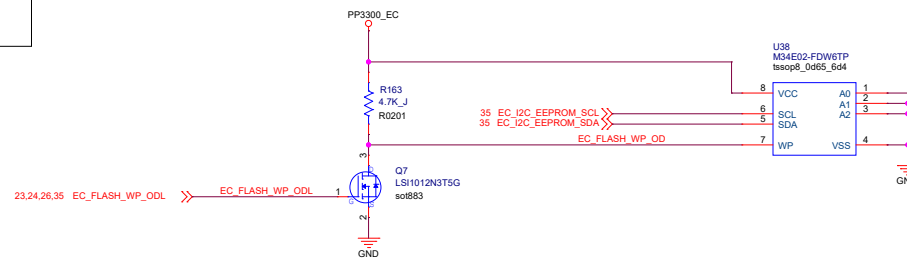
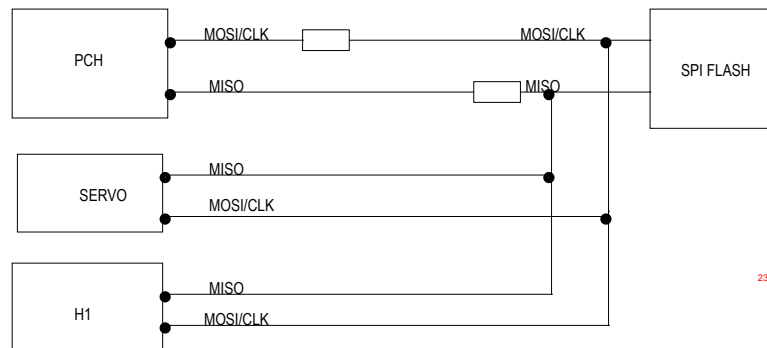
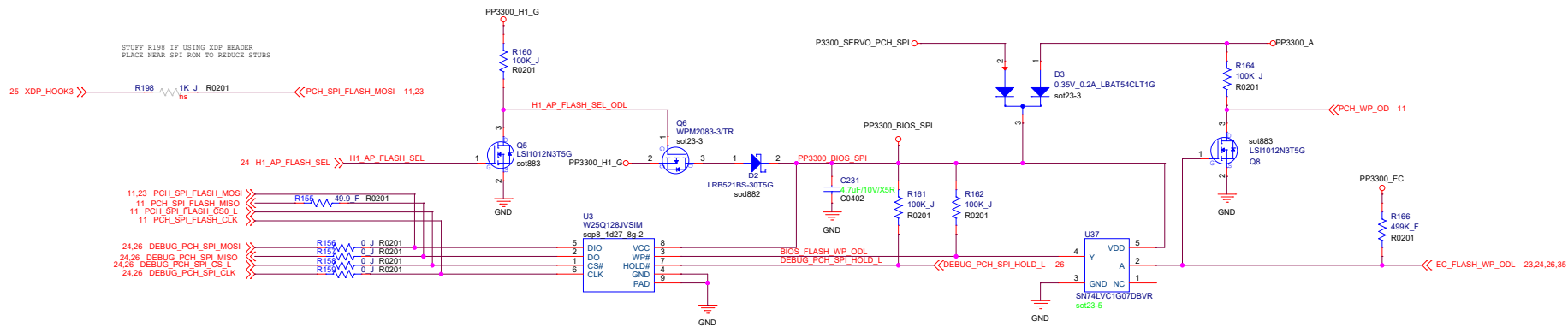


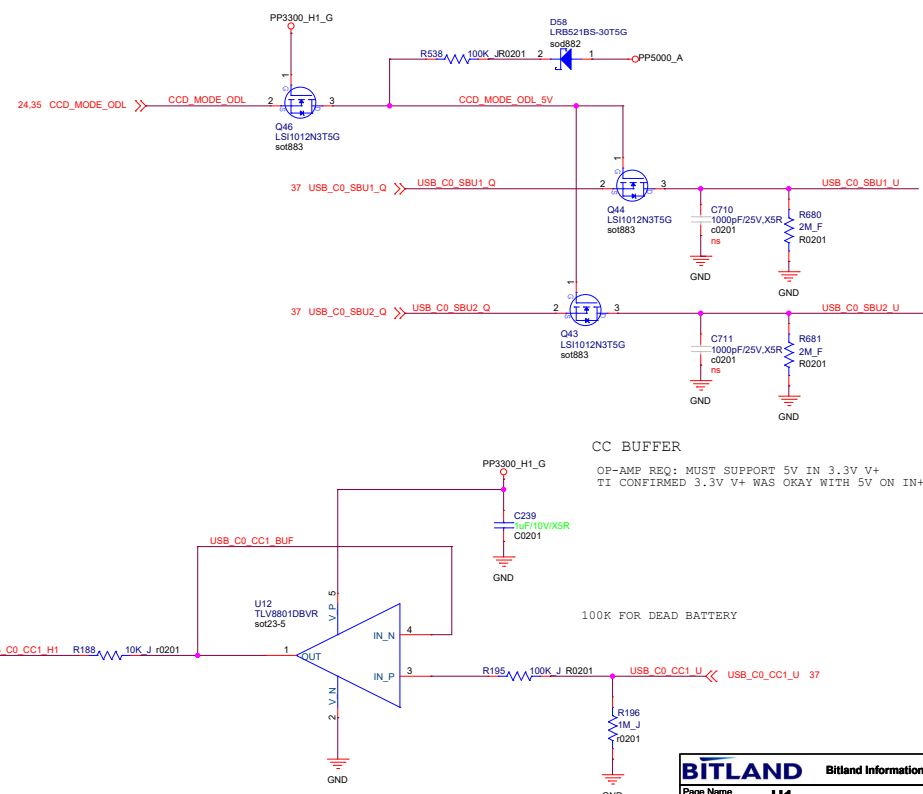












## STRAPS

STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	1M PU
H1_STRAP0	1M PU

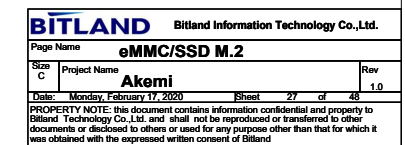
OP-AMP REQ: MUST SUPPORT 5V IN 3.3V V+  
TI CONFIRMED 3.3V V+ WAS OKAY WITH 5V ON IN+ WITH 100K

100K FOR DEAD BATTERY



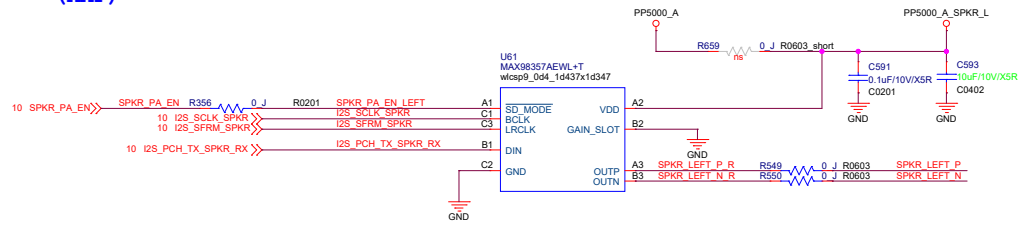






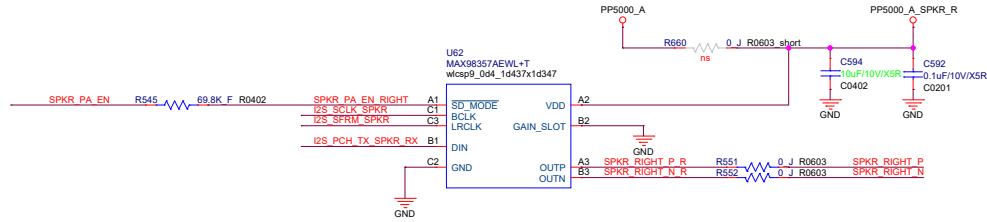
(AMP)

## LEFT CHANNEL

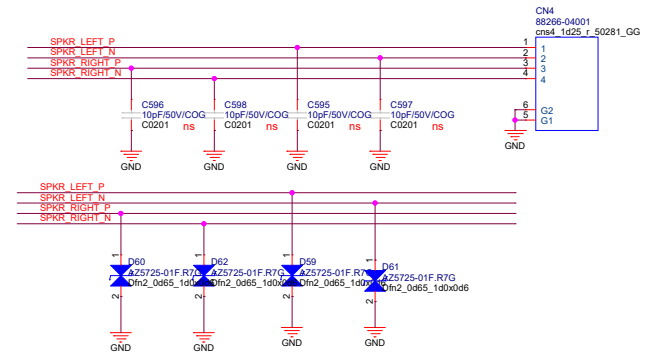


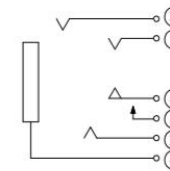
LEFT CHANNEL = SHORT (OR 2K FOR SAFETY) TO 1.8V  
GAIN\_SLOT: 100K TO GND = 15 DB GAIN  
GAIN\_SLOT: UNCONNECTED = 9 DB GAIN  
GAIN\_SLOT: 0 TO VDD = 6 DB GAIN  
GAIN\_SLOT: 0 TO GND = 12 DB GAIN  
GAIN\_SLOT: 100K TO VDD = 3 DB GAIN

## RIGHT CHANNEL



RIGHT CHANNEL = 69.8K TO 1.8V  
GAIN\_SLOT: GND = 12 DB GAIN

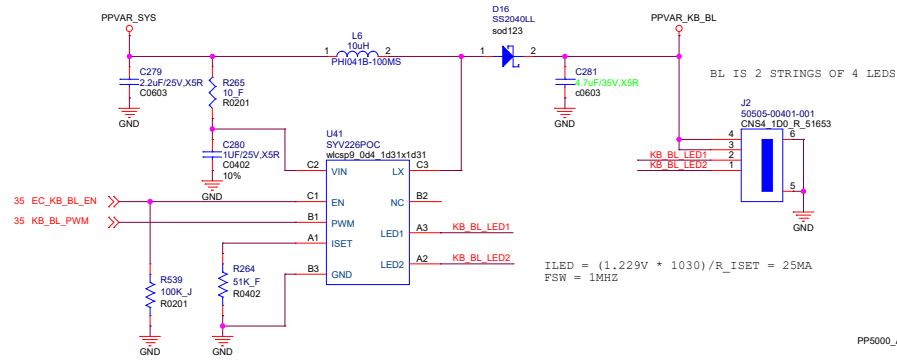




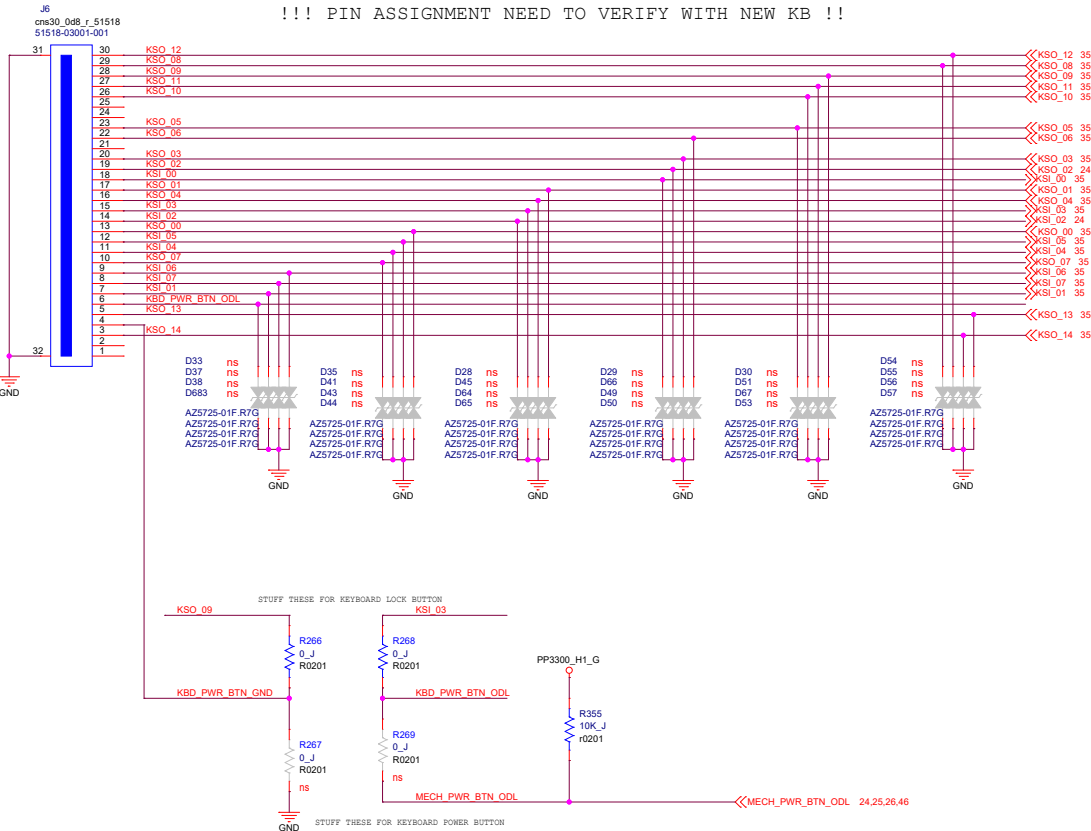
电原理图



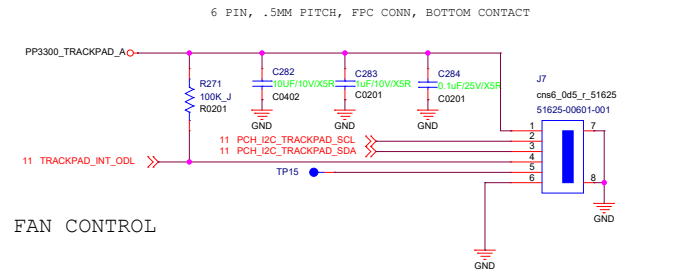
## KEYBOARD BACKLIGHT



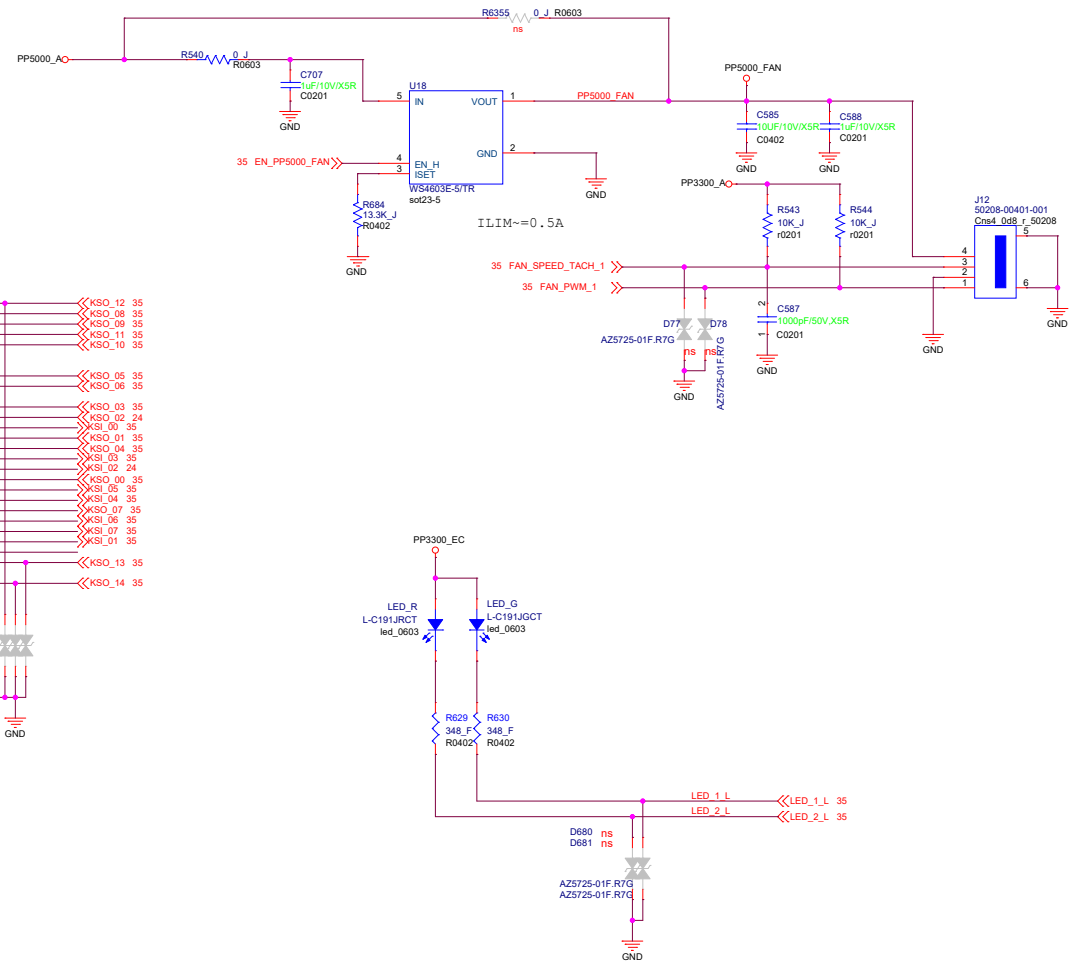
!!! PIN ASSIGNMENT NEED TO VERIFY WITH NEW KB !!




## TRACKPAD CONNECTOR



## FAN CONTROL



Remove FINGERPRINT

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FINGER PRINT SENSOR

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Akemi

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Yuesday, December 03, 2019

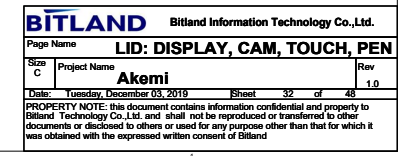
Sheet

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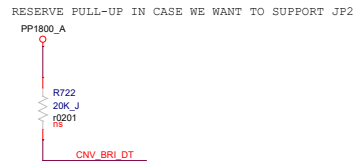
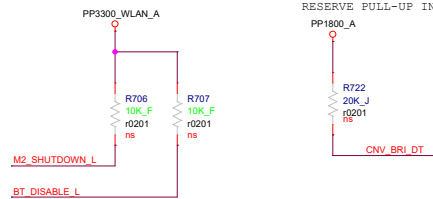
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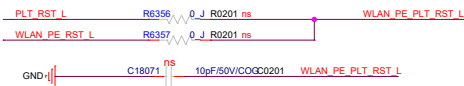
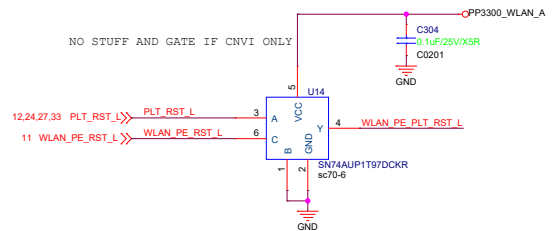
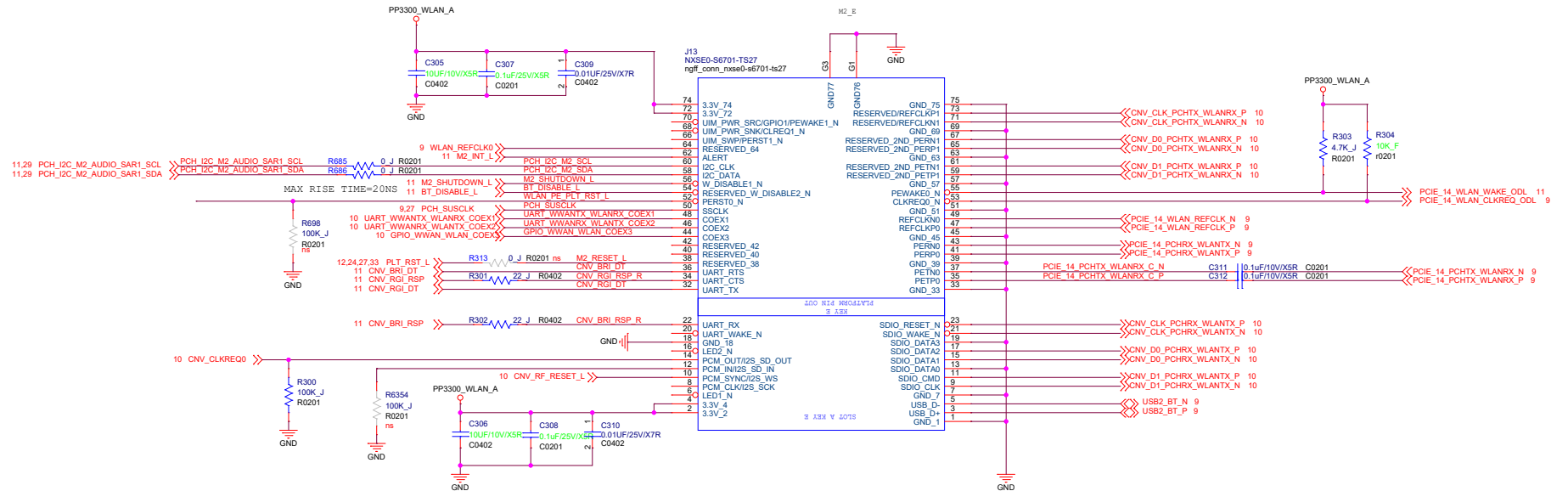
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PP3300\_WLAN\_A RISE TIME<10MS



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1.0

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Tuesday, December 03, 2019

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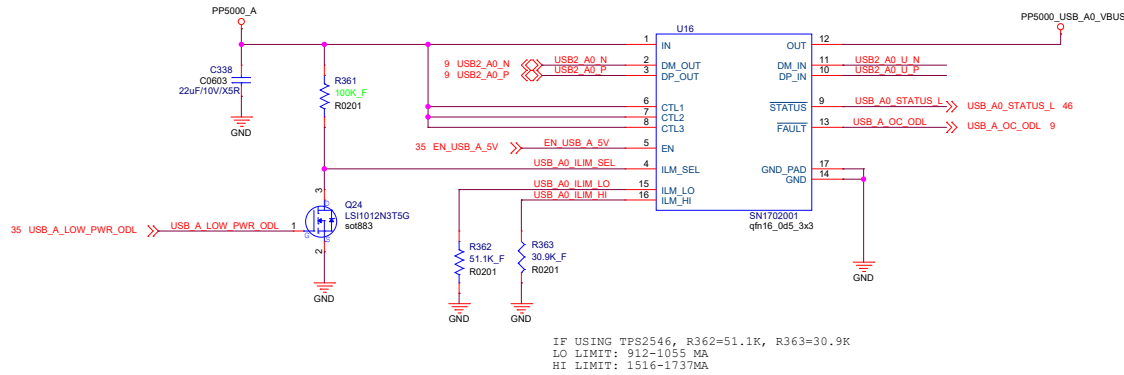
of

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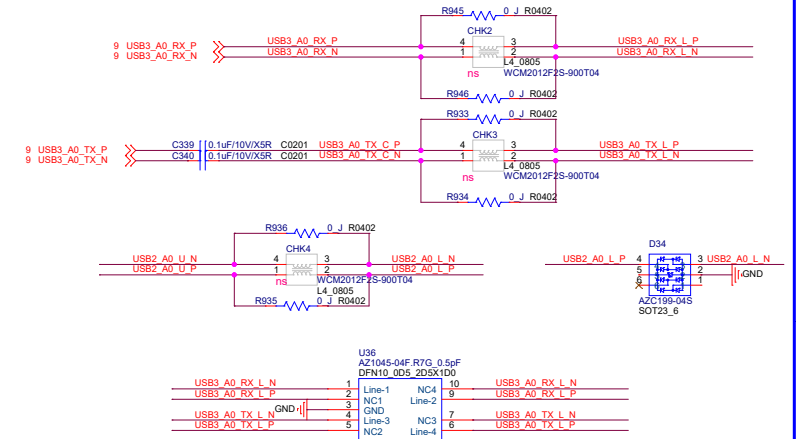
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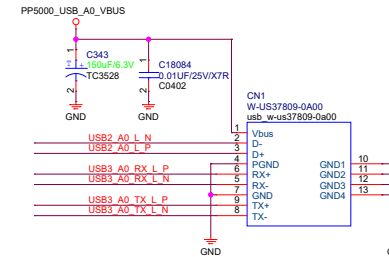
## TYPE-A:PORT 0



Deviation  
Change L5(PCMF3USB3S) to discrete EMI filter and ESD---0315

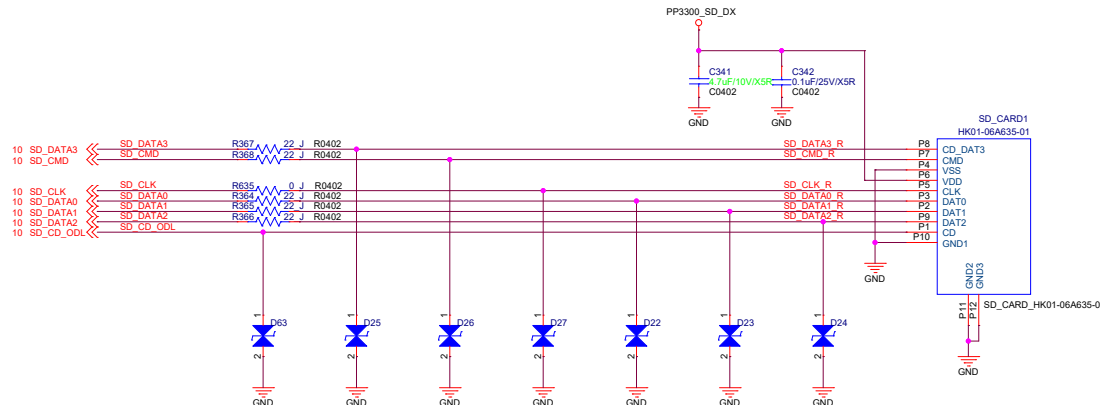


CM TO CHOOSE CONNECTOR

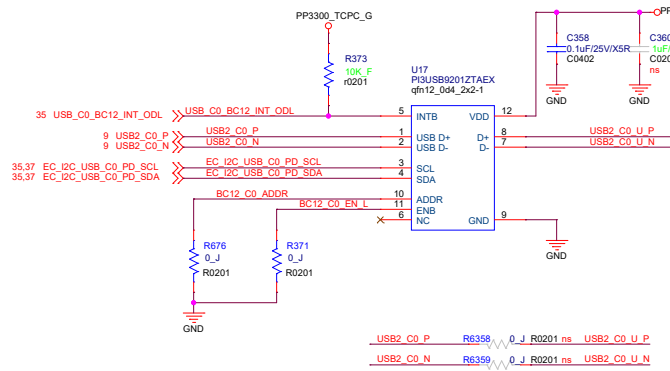


## MICRO SD CARD

\*IF NOT ON MLB, USB TO SD INTERFACE MUST BE USED

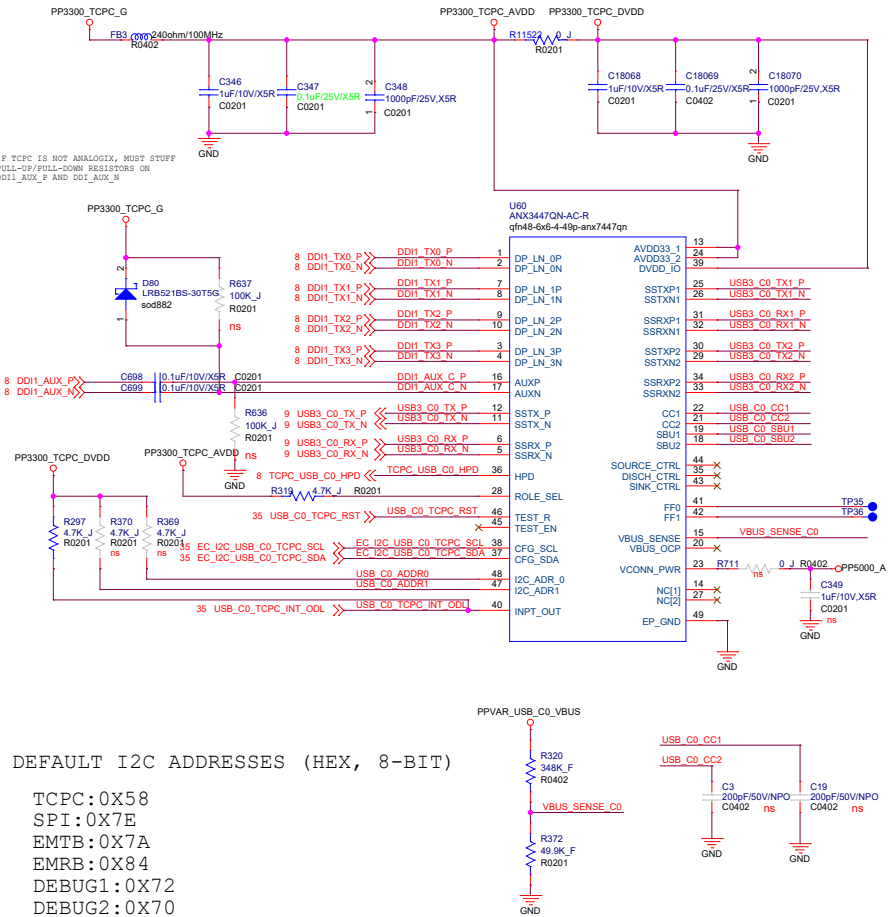


## BC1.2

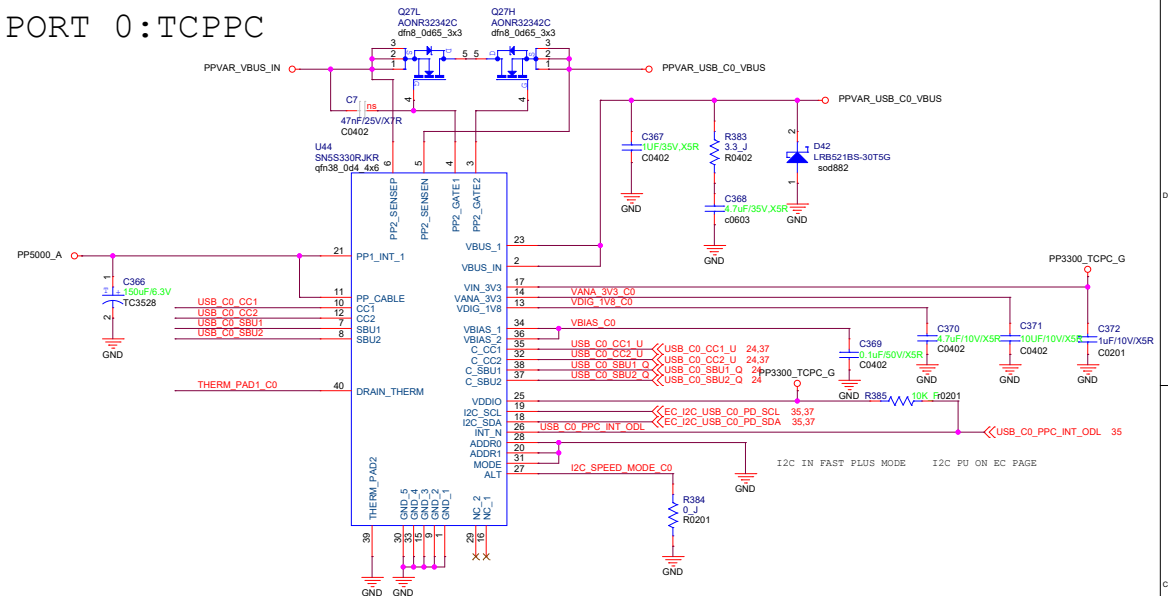


ADDRESS (HEX, 8 BIT) : 0XBE

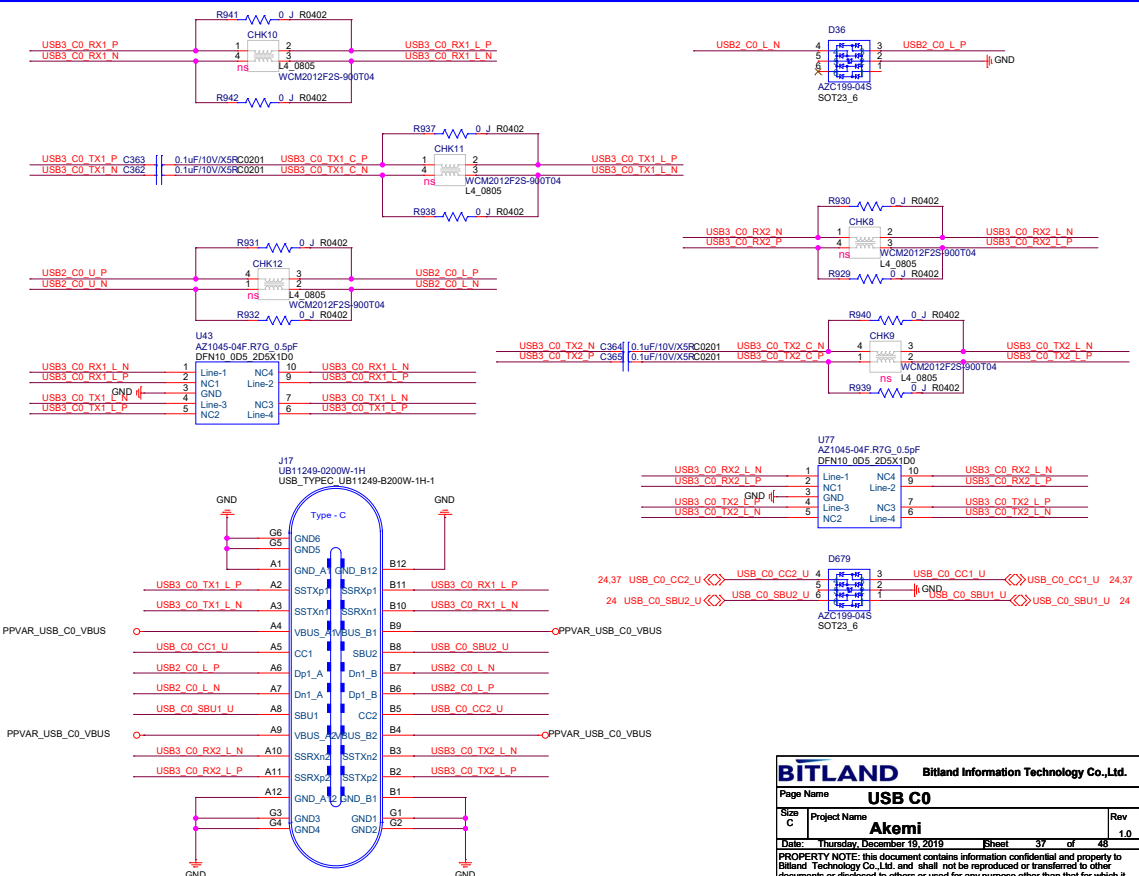
## PORT 0:TCPC



## PORT 0:TCPPC



THERM PAD 1 MUST BE CONNECTED TO ISOLATED THERMAL PAD ADDRESS (HEX, 8 BIT): 0X80

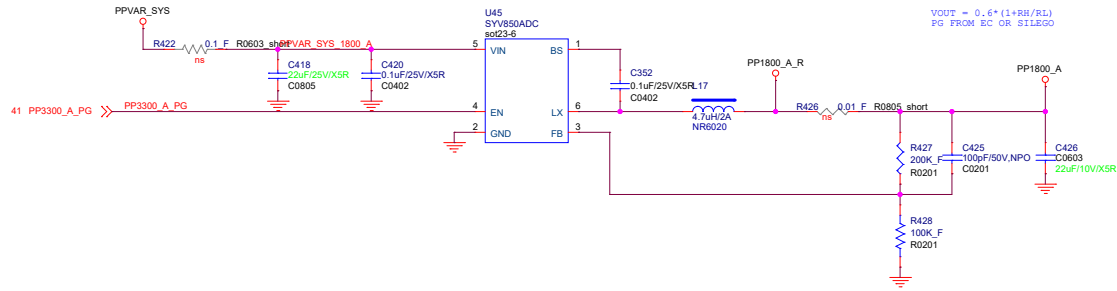




SELECT GAIN VIA I2C (0.25UA/W OR 1UA/W)

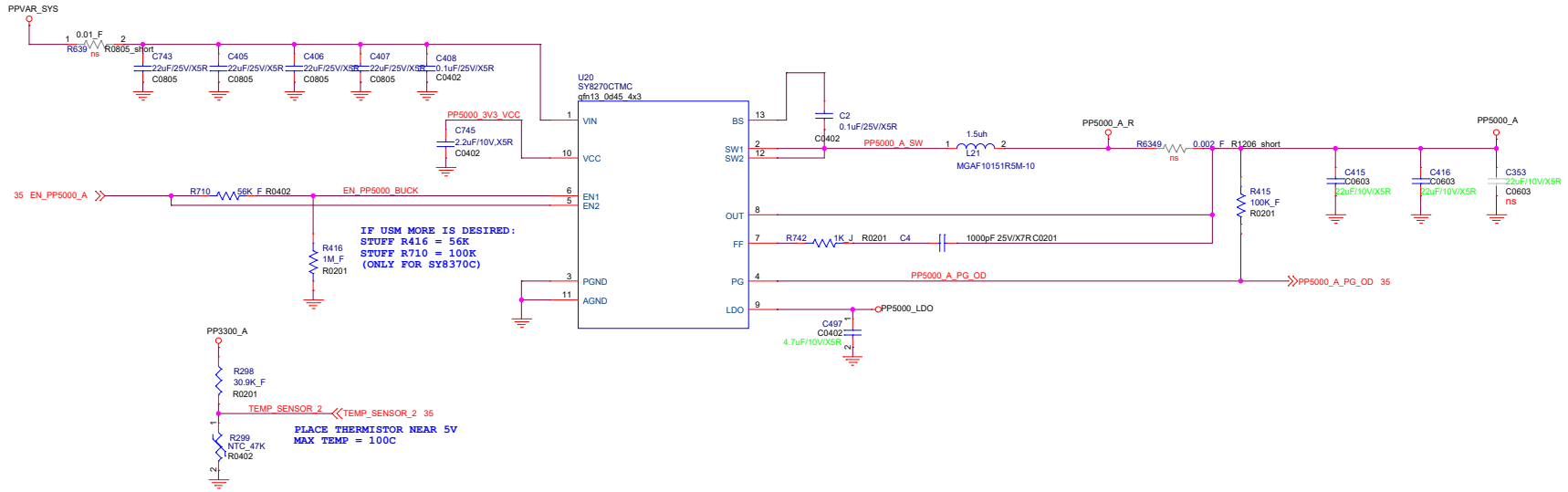
<b>BITLAND</b>		Bitland Information Technology Co.,Ltd.	
Page Name		<b>POWER:BATTERY CHARGER</b>	
Size C	Project Name <b>Akemi</b>	Rev	1.0
Date:	Tuesday, December 03, 2019	Sheet	38 of 48
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PP1800\_A  
IMAX = 0.2A  
ISAT = 0.2A  
FSW = 500KHZ

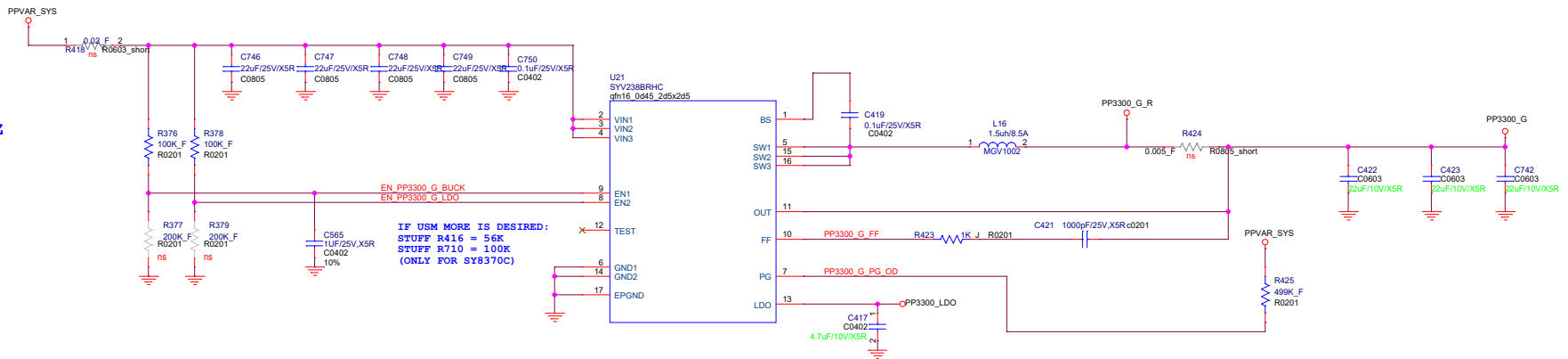


VOUT = 0.6 \* (1 + RH/RL)  
PG FROM EC OR SILEGO

PP5000\_A  
IMAX = 9.6A  
ISAT = 10.9A  
FSW = 600KHZ



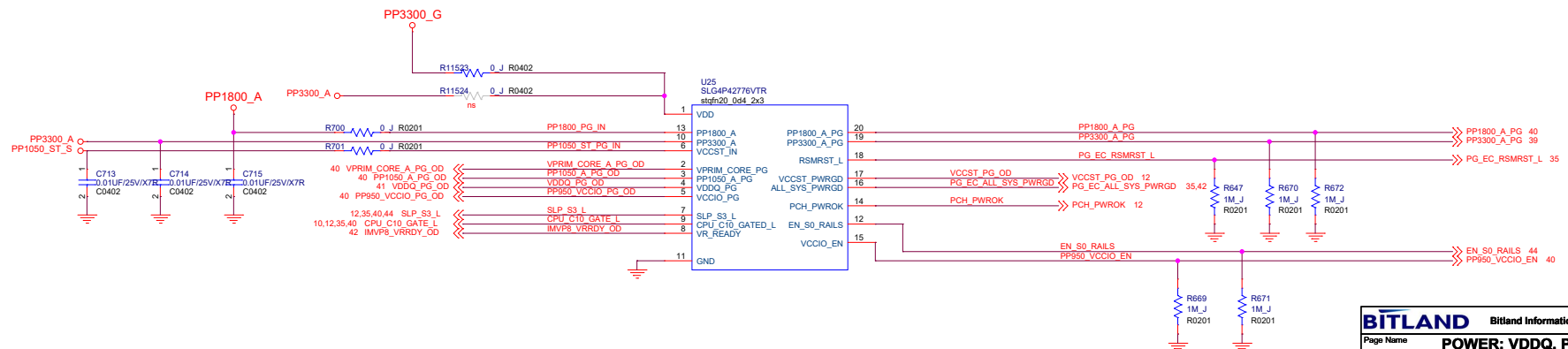
PP3300\_G  
IMAX = 7.0A  
ISAT = 8.3A  
FSW = 600KHZ



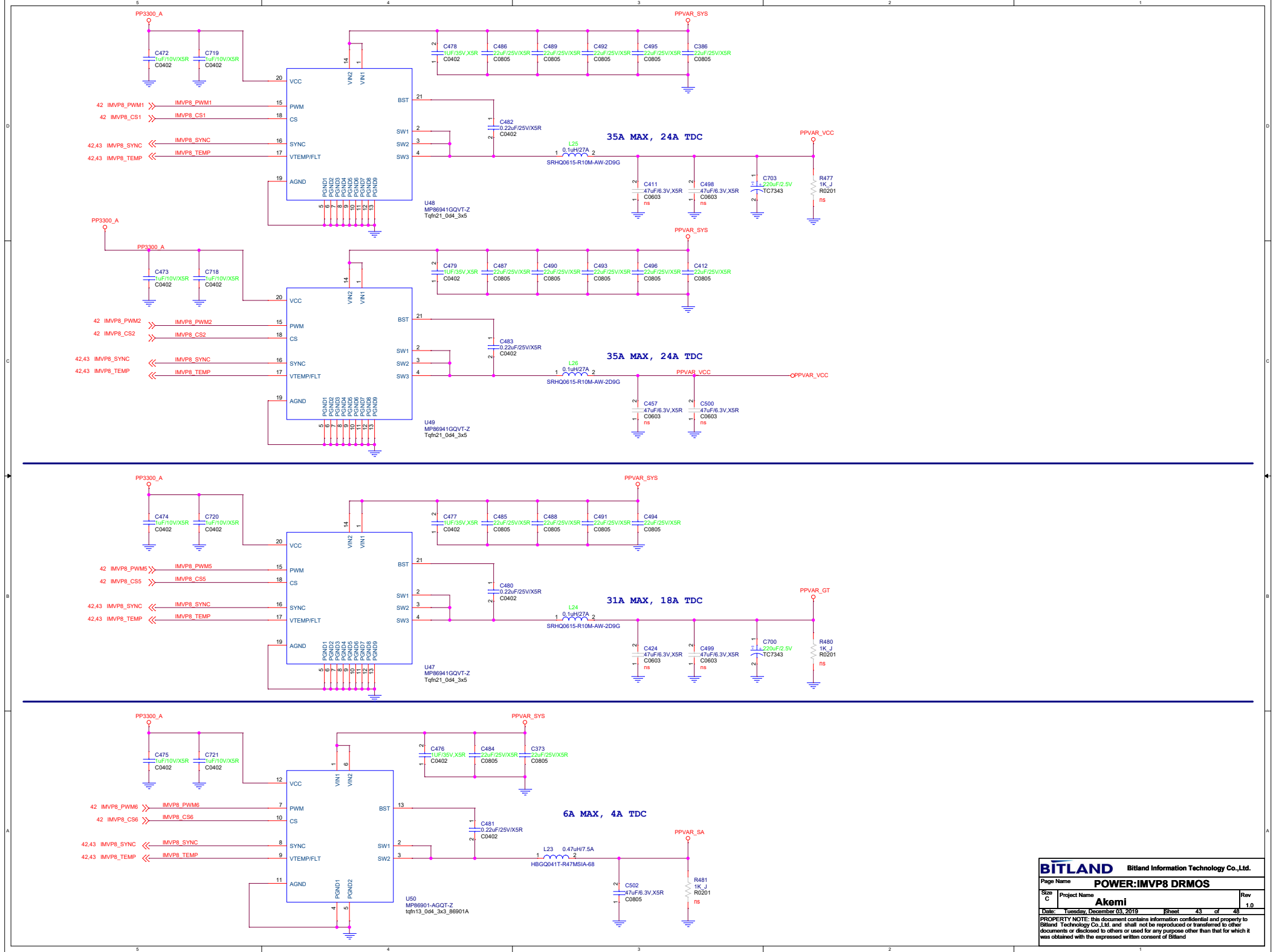


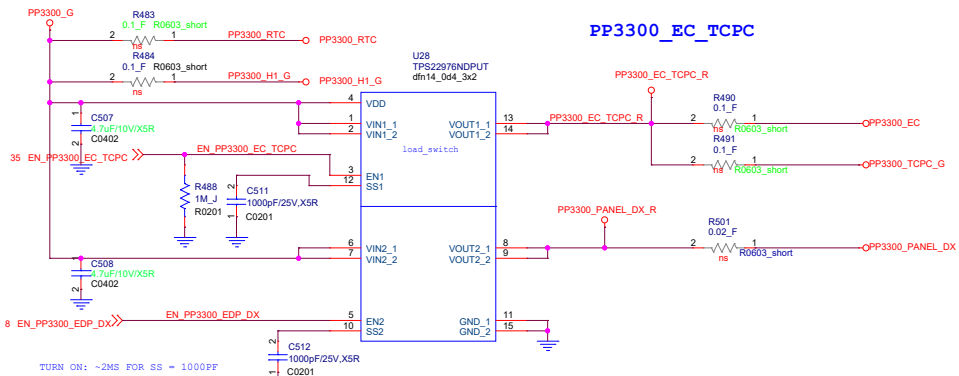


## POWER GOOD GENERATION

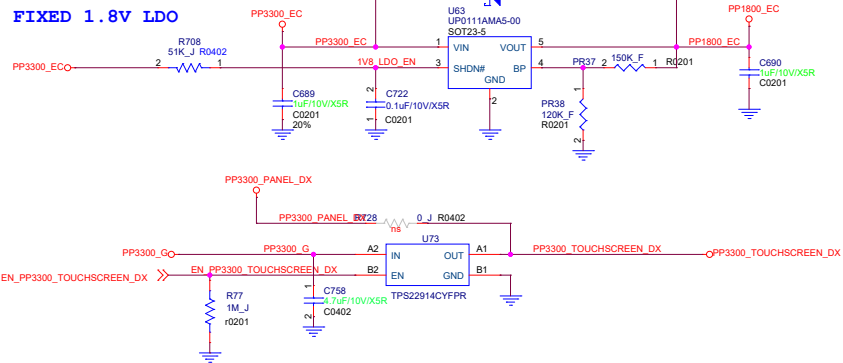




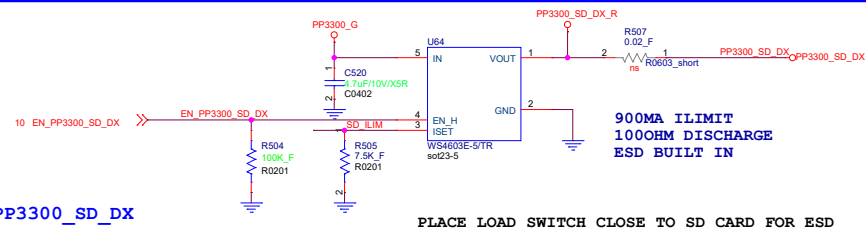




## FIXED 1.8V LDO

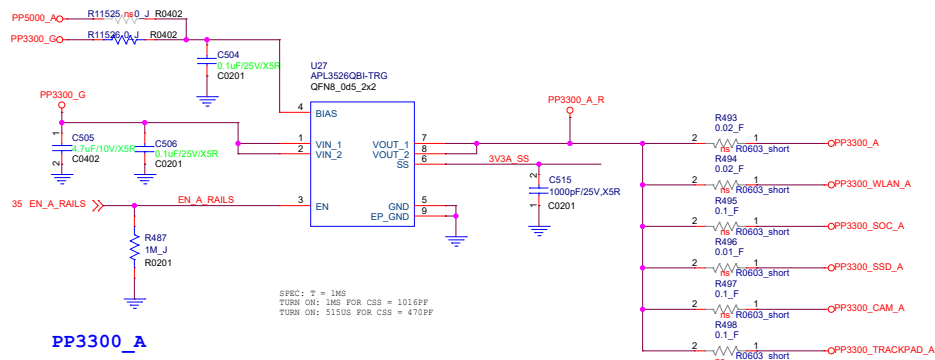


## PP3300\_SD\_DX

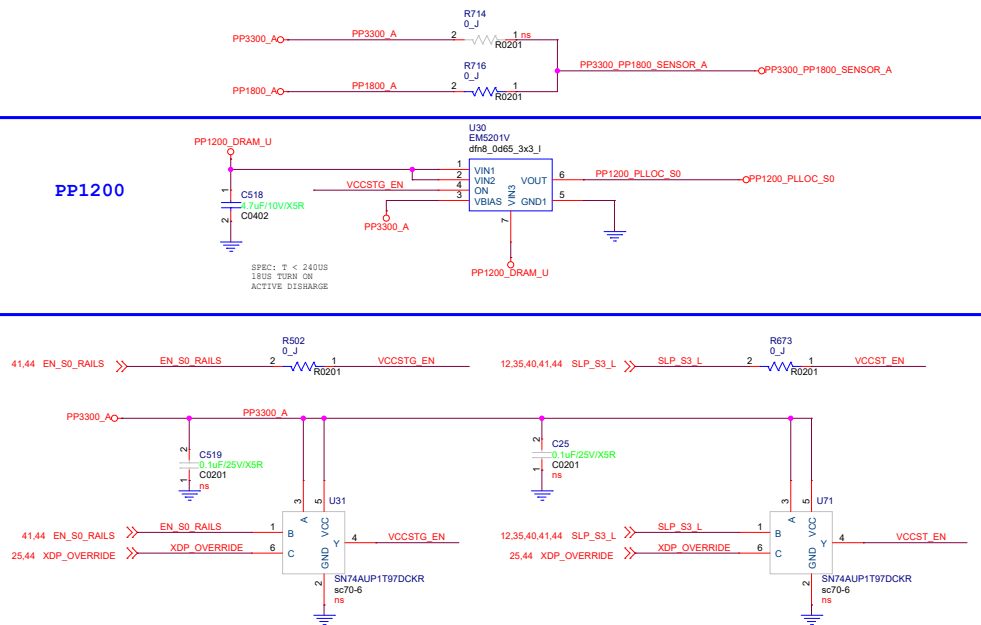


PLACE LOAD SWITCH CLOSE TO SD CARD FOR ESD

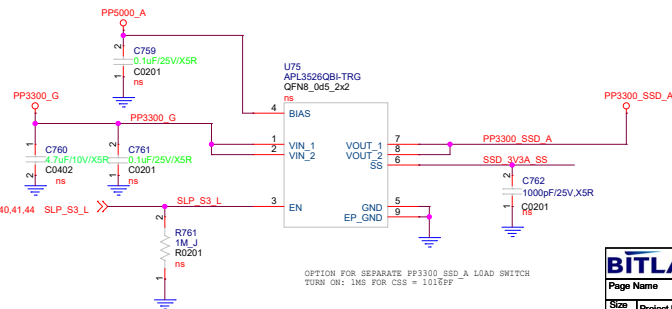
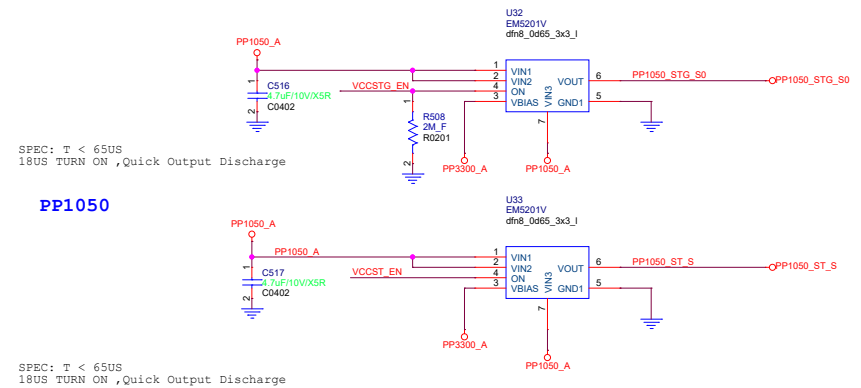
## PP3300\_A



## PP1200

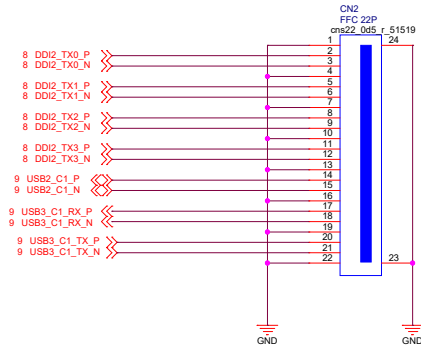
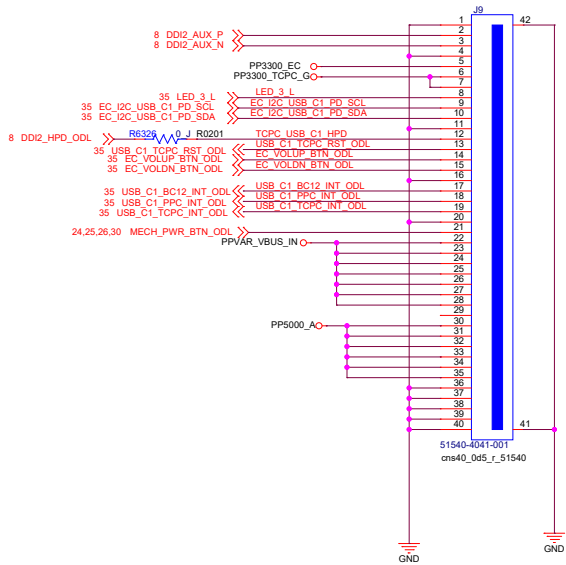
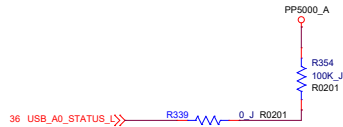


## PP1050



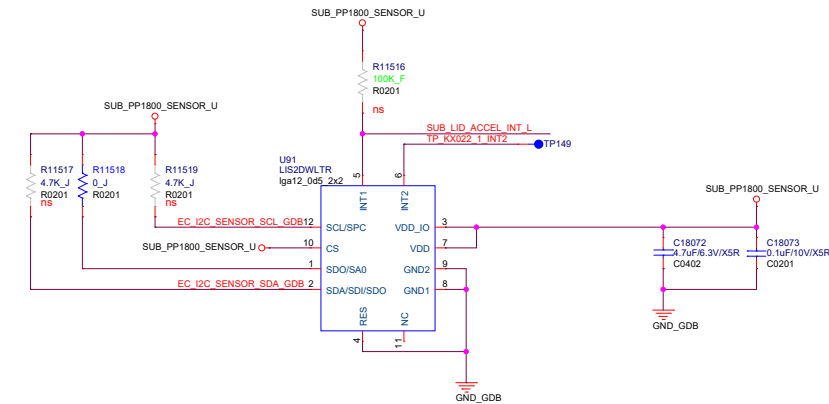
BITLAND Bitland Information Technology Co.,Ltd.			
Page Name		POWER:LOAD SWITCH	
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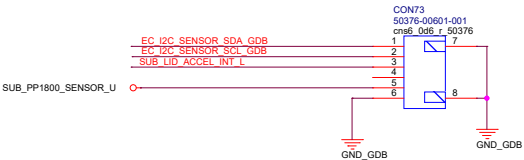


0.7A PER PIN  
5V: 5A  
PPVIR\_VBUS\_IN: 3A  
PP3300\_TPC\_G: <.7A  
PP3300\_MST: <.7A  
PP3300\_H1\_G: <.7A

LID ACCEL-CORAL  
(SUB BOARD)




I2C MODE: ( SET BY NCS TIE TO VDDIO )  
I2C ADDRESS: 0X1E (SDO\_ADDR = GND), 0X1F (SDO\_ADDR = VDDIO)  
I2C MAX SPEED = 3.4MHz



5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

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